Design Challenges in Multi-GHz RF Frequency Synthesizers

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Abstract

Today's boom in highly integrated RF tuners and transceivers requires fully-integrated, low phase noise and low spurious tones frequency synthesizers, capable of operating at multi-GHz frequencies, while tolerating the noisy environment of large mixed analog-digital ICs. Both block level and system level performance optimization and design techniques are presented.

This tutorial covers the following items: Introduction to RF PLL frequency synthesizers,

- Low phase noise crystal oscillators
- Reducing the supply injected spurs in the reference clock squaring buffer
- Fast reset phase-frequency detectors for low reference spurs
- Dynamic current matching charge-pumps for static phase offset and reference spurs reduction
- On-chip loop filters achieving low noise and low spurious tones performance
  - Capacitor Miller multiplication
  - Active feed-forward filter
  - Passive feed-forward filter
  - Sampled-mode filter
- Multi-GHz oscillators
  - Ring oscillators for wideband applications
  - LC-VCO for narrowband applications
- High speed clock buffers with stable 50% duty cycle
- Multi-GHz frequency dividers
- PLL phase noise analysis and optimization
- Power supply partitioning and filtering for reduced supply injected spurs in large mixed signal ICs
- Process and divider modulus independence of the PLL loop damping factor and bandwidth

Biography

Adrian Maxim was born in Iasi, Romania in 1968. He received the B.S.E.E. degree (with honors) in 1992 and the M.S.E.E. degree in 1994 from the Technical University of Iasi, Romania. He received the Ph.D. degree (1998) from the Technical University of Iasi, Romania and the
National Polytechnic Institute of Toulouse, France for his work on SPICE macromodeling of semiconductor devices. He has received the Leopold Escande award for outstanding Ph.D in electrical engineering from the National Polytechnic Institute of Toulouse, France. Dr. Maxim was an Assistant Professor (1992-1994) and then a Teaching Professor (1994-1998) at the Technical University of Iasi, Romania, Department of Electronics and Telecommunications, where he was involved in research on power semiconductor devices physics and modeling. During 1998 he was an Invited Professor at the National Polytechnic Institute of Toulouse, France. From 1998 to 2001 he was with Crystal Semiconductor Division of Cirrus Logic, Austin TX as a Senior mixed analog-digital design engineer and worked on multi-GHz frequency synthesizers for large mixed analog-digital ICs. From 2001 to 2004 he was with Maxim Integrated Products as a Senior Member of Technical Staff in the Fiber Optic Division, designing ICs for 10Gbps optical links and clocking applications. Dr. Maxim is now with Silicon Laboratories, Austin TX as a Senior RF design engineer working on RF tuners and transceivers. His research interests are in advanced PLL synthesizer and RF front-end architectures for wireless and wireline applications. He authored three books on SPICE modeling of semiconductor devices and circuits and over 50 technical papers in IEEE Journals and Conferences. Dr. Maxim is a technical reviewer for the IEEE International Symposium on Circuits and Systems (ISCAS) and the IEEE International Symposium on Signals Circuits and Systems (ISSCS).

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