A 4 µA-Quiescent-Current Dual-Mode Digitally-Controlled Buck Converter IC for Cellular Phone Applications

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Outline

• Application requirements
• Dual-mode controller
• Analog and digital interface
• Internal power management
• Experimental results
• Summary
Motivation

- Low quiescent current to extend standby time
- Integrate with digital systems on same die
- Easy interface with digital systems $\rightarrow$ fast response with digital feed forward
- Computation capability for advanced control schemes (e.g. adaptive control)
- Immunity to analog component variations and noise
- Benefit from technology scaling, easier to migrate to new technology
Buck Converter Requirements In Cell Phones

- Convert battery voltage to high quality DC voltage
- High efficiency over wide load range
  - Pulse Width Modulation (PWM) for heavy load
  - Pulse Frequency Modulation (PFM) for light load
- Low quiescent current in PFM
Typical Handset Power Management Diagram

Battery

\[ V_{\text{in}}: 5.5-2.8 \text{ V} \]

Buck converter system

\[ V_x \]

\[ L \]

\[ C \]

\[ V_o \]

Controller

\[ V_{\text{ref}} \]

Cellular phone chip set

\[ V_o: 1.0-1.8 \text{ V}, \text{ tolerance 2-3\%} \]

\[ I_o: 0-400 \text{ mA} \]

\[ I_o \]

Ctrl (PWM)

Ctrl (PFM)
DC-DC Converter Modes of Operation

Continuous conduction

Discontinuous conduction

\[ T_s = \frac{1}{f_s} \]
DC-DC Converter Losses

- Conduction loss
- Switching loss
- Controller quiescent power
- Misc: output inductor core loss, stray inductance loss, etc
# PWM and PFM Control

<table>
<thead>
<tr>
<th></th>
<th>Switching freq.</th>
<th>Losses</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PWM</strong></td>
<td>Constant</td>
<td>Conduction loss and switching loss</td>
</tr>
<tr>
<td><strong>PFM</strong></td>
<td>Proportional to load current</td>
<td>Conduction loss and switching loss scale with load, controller quiescent current significant at light load</td>
</tr>
</tbody>
</table>

![Circuit Diagram]

- **V**<sub>in</sub>:
  - Input voltage
- **V**<sub>ref</sub>:
  - Reference voltage
- **V**<sub>x</sub>:
  - Intermediate voltage
- **L**:
  - Inductor
- **C**:
  - Capacitor
- **V**<sub>o</sub>:
  - Output voltage

**Notes:**
- Conduction loss and switching loss scale with load, controller quiescent current significant at light load.
PWM and PFM Losses

- Conduction loss
- Switching loss

Controller quiescent power

PFM, standby mode

PWM, talk mode
• Dual mode controller
• Digital Pulse Width Modulator (DPWM)
• Power switches
PFM Mode Diagram & Switching Behavior

- Converter discontinuous conduction
- Fixed on-time control
- Zero-DC-bias comparator for low power
PFM Mode Comparator

PWM Mode

0.5-1.5 MHz switching frequency

Buck converter IC

Comparator

PFM mode

PFM logic

Digital dither

PID

MUX

Ring osc

Simplified power train

system clock

V_{in}

V_{x}

L

C

V_{o}

V_{o}

V_{ref}

D_{e}

MODE

GND

V_{in}

V_{x}

V_{o}

Vin

GNDMODE

0.5-1.5 MHz switching frequency

Buck converter IC

Comparator

PFM mode

PFM logic

Digital dither

PID

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Simplified power train

system clock

V_{in}

V_{x}

L

C

V_{o}

V_{o}

V_{ref}

D_{e}

MODE

GND

V_{ref}

V_{o}

V_{o}

V_{ref}

D_{e}

MODE

GND

PWM Mode ADC Considerations

- Windowed quantization range
- Tolerance to switching noise and switching ripple
- Digital implementation
Ring Oscillator with Subthreshold Bias

Linear dependency of ring-oscillator frequency on bias current

Current-starved differential ring oscillator

![Diagram of ring oscillator with bias current](image)

![Graph showing linear dependency of frequency on bias current](graph)
PWM Mode Ring-ADC Architecture

- $\Delta V \rightarrow \Delta I \rightarrow \Delta f \rightarrow D_e$
- Windowed quantization range
- Insensitive to switching noise
- bulk part synthesizable

- Automatic monotonicity
- Wide Vo operating range
- 16 mV/step, 80 mV window, 0.15mm$^2$ on 0.25 μm CMOS
DPWM

- Ring-MUX scheme
- 5-bit DPWM hardware + 5-bit digital dither
- 1 μA at 600 kHz

1. A. Peterchev “Quantization resolution and limit cycling in digitally controlled PWM converters”
Power Train and Internal Power Management

• Low break down voltage → Cascoded power switches & internal linear regulator

• Scavenges $I_p$ from high-side gate drive discharge

![Diagram of power train and internal power management system](image)
Experimental Results

- Load transient responses
- Steady state response
- Efficiency
- Chip micrograph
Load Transient Response

Vin = 3.2 V, Vo = 1.2 V. Load step 100 mA

- PWM mode: both steady-state voltages in ADC zero-error bin

- PFM mode: voltage ripple <25mV @100 mA
Steady-state Response: PWM Mode

Vin = 3.2 V, Vo = 1.2 V, fs = 500 kHz.
Efficiency: PWM and PFM Modes

Vin = 4.5 V
Vo = 1.5 V.

- PWM efficiency drops off at low Io
- PFM efficiency high at low Io
- Composite efficiency high over wide Io range
Summary of Chip Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25-μm CMOS (Max. supply 2.75 V)</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>5.5-2.8 V</td>
</tr>
<tr>
<td>Output voltage range</td>
<td>1-1.8 V</td>
</tr>
<tr>
<td>External LC filter</td>
<td>L=10 μH, C=47 μF</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>400 mA</td>
</tr>
<tr>
<td>PFM mode sampling frequency</td>
<td>600 kHz</td>
</tr>
<tr>
<td>PFM mode quiescent current</td>
<td>4 μA</td>
</tr>
<tr>
<td>PWM mode switching frequency</td>
<td>0.5-1.5 MHz</td>
</tr>
<tr>
<td>PWM mode DC output voltage precision</td>
<td>±0.8%</td>
</tr>
<tr>
<td>PWM mode output voltage ripple</td>
<td>2 mV</td>
</tr>
<tr>
<td>Active chip area</td>
<td>2 mm²</td>
</tr>
</tbody>
</table>
Chip Micrograph

Active area 2 mm²

Controller

Power train
Summary

• Efficient digital control for mass market power management

• More than 3-fold quiescent current reduction

• Low-power and robust analog-digital interface

• Controller + Power train on low-voltage CMOS process
Acknowledgement

• Funding provided by Linear Technology, Fairchild Semiconductor, National Semiconductor, and California Micro Program
PWM Mode: Quantization Resolutions

**Problem:** Steady state oscillation — limit cycles

**Solution:** Multiple DPWM bins in ADC zero error bin