Modeling and Characterization of Contact-Edge Roughness for Minimizing Design and Manufacturing Variations in 32-nm Node Standard Cell

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ABSTRACT

Despite intensive attention on line-edge roughness (LER), contact-edge roughness (CER) has been relatively less studied. Contact patterning is one of the critical steps in a state-of-the-art lithography process; meanwhile, the design rule shrinking leads to larger CER in contact holes. Since source/drain (S/D) contact resistance depend on contact area and shape, larger CER results in significant change in a device current. In this paper, we first propose a CER model based on power spectral density function which is a function of RMS edge roughness, correlation length, and fractal dimension. Then, we present a comprehensive contact extraction methodology for analyzing process-induced CER effects on circuit performance. In our new contact extraction model, we first dissect the contact with a same distance, and then calculate the effective resistance considering both the shape weighting factor and the distance weighting factor for stress induced CMOS cells. Using the results of CER, we analyze the impact of CER variation on the S/D contact resistance and the device saturation current. Results show that when the rms value of CER is $10nm$, the S/D contact resistance and the device saturation current can vary by as much as 57.8% and 2.1%, respectively.

Keywords: Contact, LER, CER, Lithography, Variation, Characterization, Standard Cell, DFM

1. INTRODUCTION

As semiconductor device dimensions have continuously scaled into the nano-meter regime, the contact printability has become one of the most critical steps in a lithography process [1–4]. The contact variation due to lithography causes the area change and the overlay problem between metal layer and silicide layer from the targeted design which leads to contact resistance variation, therefore, transistor performance degradation [1, 4].

There are two types of lithography variations that cause undesirable performance mismatch in identically designed transistor: *systematic variation* and *random variation*. The systematic lithography variation for contact patterning is caused by deterministic pattern proximity which comes from the limitation of a lithography equipment. Even if many researchers have been working in resolution enhancement techniques (RET) such as optical proximity correction (OPC), phase shifting mask (PSM), off-axis illumination (OAI) etc, lithographic variation still continues to be a challenge [5, 6]. As shown in Figure 1(a), the lithography proximity makes the contact pattern rounded due to the limitation and variation of a lithography equipment. Lithography process with the systematic variation is defined by a set of defocus and exposure levels. Even for nominal defocus and exposure levels, printing of small geometries results in loss of image quality [7, 8]. This causes distorted non-rectangular shapes of the geometries in S/D contact layer.

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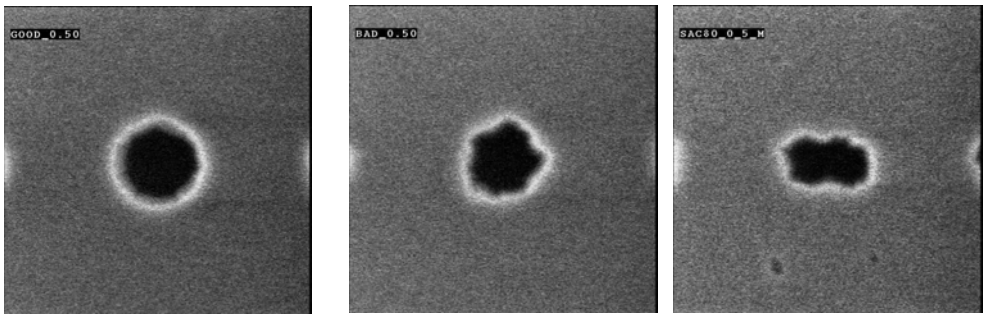


(a) Lithographic proximity (b) Systematic & random CER variation

Figure 1. Lithographic variations for contact [10].

The random lithography variation, e.g., LER (line-edge roughness) for a line patterning and CER (contact-edge roughness) for a contact patterning, becomes more important in sub-32nm node devices [9, 10]. That is because a patterned photo-resist (PR) layer used to produce such small feature sizes typically has a high aspect ratio, and maintaining a desired CD (critical dimension) can be very difficult due to small process margin [5, 6]. Despite intensive attention on LER, CER has been relatively less studied even though contact patterning is one of the most difficult lithography processes. As the aggressive scaling continues into the nanometer regime, CER does not scale accordingly and becomes an increasingly larger fraction of the contact pattern [11–13].

Geometrically, CER caused by lithography process variation brings both the edge roughness and the area change of a contact pattern [10,13] as shown in Firgure 1(b), which may result in the change of contact resistance and even the current degradation. According to the experimental results in the $32nm$ contact manufacturing, if the 3 σ roughness of CER is $4nm$, then the area variation (3 σ) could be more than $48nm^2$ which is as much as 10% of the total contact area.

Moreover, if the systematic lithography variation, i.e., dosage and focus, is also added in the contact patterning, the contact area variation would be much more. The paper [4] shows that the variation of contact-resistance is up to 50% in $65nm$ design when the systematic and the random variations are considered on manufacturing process. Thus we can easily guess that the variation could be higher in $32nm$ devices because the portion of systematic and random contact variation becomes much larger than that of $65nm$ devices in a whole contact area.

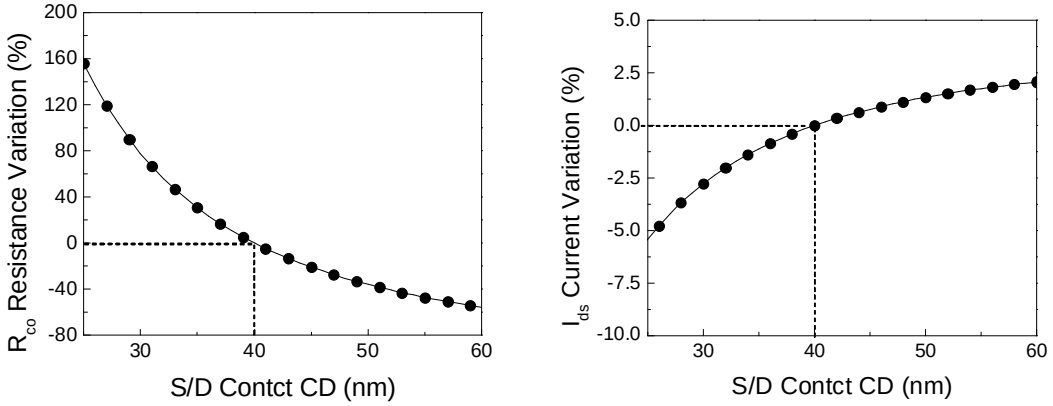
In this paper we propose a CER model and a comprehensive contact layout extraction method for analyzing process-induced CER effects on circuit performance. Our approach is mainly based on the new SPICE-level compact model for S/D contact layout. The objective of the proposed CER model and the extraction method is to understand the impact of contact variation on circuit performance and to give a guide for robust design of standard cell layouts. The major contributions of this paper include the following:

- We propose a CER model based on the power spectral density model which is a function of RMS edge roughness, correlation length, and fractal dimension.
- We present the first systematic study on the impact of contact shape on the device saturation current, and propose a simple yet effective model to estimate the performance impact of S/D contacts. Our model considers contact distance from gate, contact shape, and contact area.
- We investigate the impact of S/D contact variation on the circuit performance in a standard cell. This is the first study for the CER-aware extraction and its timing impact.

The rest of the paper is organized as follows. Section 2 describes the sources of S/D contact variation and the timing impact. Section 3 presents our CER model. Section 4 presents the new compact model and its validation. Experimental results are discussed in Section 5, followed by conclusions in Section 6.

2. IMPACT OF S/D CONTACT VARIATION

Since the lithography tools have remained at $193nm$ even with technology scaling below $32nm$ resulting in significant variations. Printing of small geometries results in loss of image quality [7], which results in distorted non-rectangular shapes of the geometries in S/D contact layer. In reality, due to the relatively small process margin, contact patterning is one of the most challenging tasks in hyper-NA (numerical aperture) lithography [5, 14]. The increased imaging challenges for advanced node contacts lead to strong off-axis illumination [15] and inverse lithography techniques [14, 16] for sub-$45nm$ node devices, which implies that the modern contact patterning still suffers from the CD and area variation due to the lithography proximity and process variation. Both variations cause the area change of contact plug which induces device performance degradation.



(a) Impact on the contact resistance

(b) Impact of the device saturation current

Figure 2. The impact of S/D contact CD variation.

Electrically, the contact area variation is highly related to the S/D device saturation current degradation. In this experiment, we used a commercial HSPICE simulator [17] by changing the source/drain contact resistances and assume that the contact resistance of NMOS and PMOS are same. The nominal contact size is $40nm$ for all standard cells. In our experiments as shown in Figure 2(a) and (b) in NMOS devices, we observe that as the S/D contact CD decreases, the S/D contact resistance dramatically increases whereas the device saturation current highly drops down. Since the parasitic S/D contact resistance is highly increased due to the smaller contact area, the portion of the contact resistance becomes higher in a total device current path from the source to the drain. The result shows that $10nm$ contact CD variation causes up to 5% degradation of the saturation current and over 100% increase of the S/D contact resistance, and the current variation is highly correlated with the contact CD variation.

3. CONTACT EDGE ROUGHNESS (CER) MODEL

Conventionally line edge roughness is represented as a function of spatial frequency through the power spectral density (PSD) function. Because SEMs or any other metrology tools measure over finite distances, the PSD $S(f)$ can be expressed as in Eq. (1):

$$S(f) = \frac{d}{N} \left| \sum_{m=-N/2}^{(N/2)-1} \left[y\left(x_m\right) - \bar{y} \right] e^{-2\pi i f x_m} \right|^2 , \tag{1}$$

where $x_m = md$. Large values of $S(f)$ indicate that there is a large amount of line-edge roughness at the spatial frequency f.

It is noted that there is no analytical PSD exists in most circumstances, and usually it is approximated as the following in Eq. (2):

$$S(f) = \frac{2\sigma_{LER}^2 L_c}{\left(1 + (2\pi)^2 f^2 L_c^2\right)^{0.5+\alpha}}, \tag{2}$$

where σ_{LER} is the standard deviation of the roughness, $f = i\frac{1}{N\Delta_z}$, and $0 \leq i \leq \frac{N}{2}$, N is the number of points along the line. The parameter L_c is referred to as the correlation length, and α is related to the fractal dimension D as $\alpha = 2 - D$. Hence, the LER for a large number of resists can be characterized by just three numbers, σ_{LER}, L_c, and α.

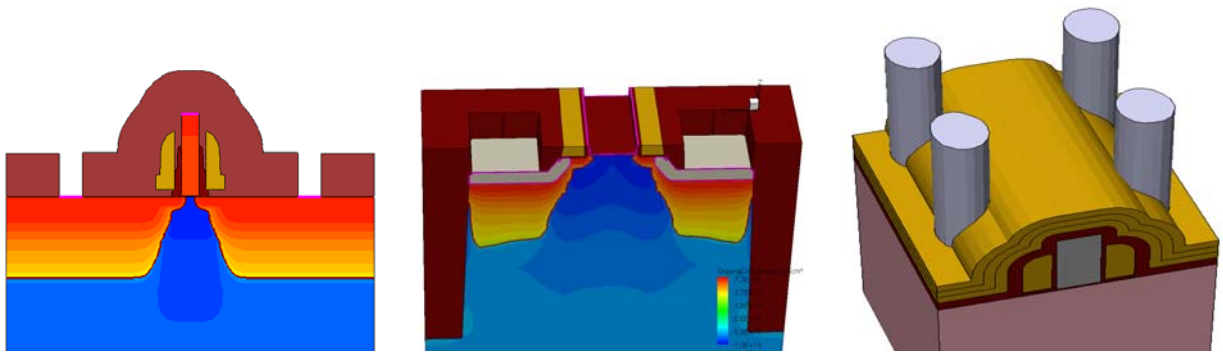
With the magnitude information provided by $S(f)$, we can reconstruct random line edges by applying a random phase to each frequency component of the PSD to form a unique signal in the frequency domain. A line edge with roughness can be simulated by doing an inverse Fourier transform of this signal. Random lines are distinguished through random phases applied. The contact roughness-formation mechanism could be different from lines, and there were not as much work done for contacts as for lines. Here, we assume the distribution of radii of a contact at angles from 0 to 2π follows the PSD mentioned as above. Hence, contacts with roughness can be reconstructed.

4. CIRCUIT LEVEL COMPACT S/D CONTACT MODEL

The lithography variation could vary the S/D contact shape, area and even distance from gate line, which causes the performance degradation. Thus, we should consider the impact of S/D contact variation on the standard cell performance in design time, which needs a new circuit level compact model of S/D contact pattern. In this section, we first illustrate the TCAD simulation of a CMOS cell in Section 4.1. Then we propose our new circuit level compact model for non-rectangular contact layout in Section 4.2.

4.1. TCAD Simulation Set-up

Sentaurus process and device simulator [18] is used to estimate impacts of the S/D contact effects on device performance, and used to verify accuracy of the our compact model for non-rectangular contact layout. To investigate the impact of S/D contact patterning displacement, we use 2D device structure of $32nm$ standard cell in Figure 3(a). Then we measure the S/D saturation current by varying the position of S/D contacts. The $32nm$ CMOS cell uses intensive stress-enhancement techniques: NMOS uses a tensile stress liner, and PMOS has a compressive stress liner and embedded SiGe in S/D region. We also use 3D TCAD simulation for looking into the impact of contact size and contact shape. We first generate printed images of contact pattern with OPC taken into account. For lithography simulation, we use a commercial lithography simulation tool [19]. The standard cell layout is converted into 3D structure for TCAD simulation with Ligament layout editor [18] as shown in Figure 3(b) and (c). To save a simulation time and memory, a quarter of the structure mesh is generated, yet the other structure is created by reflection.

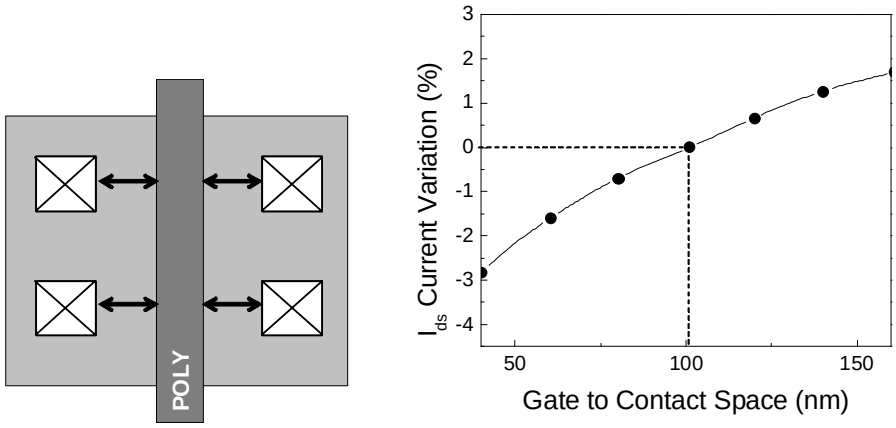


(a) 2D TCAD structure (b) 3D TCAD structure (c) 3D structure from print-images

Figure 3. Structural view of TCAD simulation.

4.2. Equivalent Contact Resistance Model

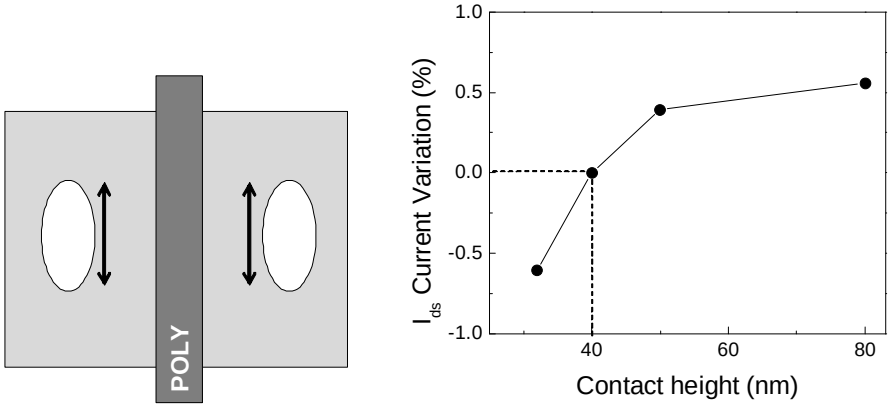
Mask overlay problem causes the displacement of the S/D contact patterning from the gate poly layer. The change of the contact position also affects the saturation current in a device. In 32-nm node standard cell, MOSFETs are used to use a stress enhancement technique in which the mobility of carriers in the substrate depends on the distance of contact and gate poly line because neighboring contacts may relax the actual strain in channel. To analyze the overlay impact due to contact pattern shifting, we use a rigorous 3D TCAD simulation tools combined with our CER-generated contact layout, and investigate the impact on the systematic and random lithographic variations on manufacturing as well as the timing and power variations on circuit performance.



(a) View of contact space to poly (b) Impact of contact position variation

Figure 4. The impact of S/D contact overlay(displacement).

According to the paper [2,20,21], the variation of the contact position causes a degradation of the saturation current in the stress induced device. This is because neighboring contact hole may locally relax the actual strain in channel. As shown in Figure 4(b) in which the results are referred from [21], the saturation current degrades as contacts are placed closer to the gate in PMOS devices. Since the mobility modulation of PMOS is different from that of NMOS, the trend of NMOS devices may be another trend. Although the current variation can be different from the input stress parameter, we can find that the current variation by the stress relaxation could be happened due to mask overlay problem.



(a) View of contact shape (b) Impact of contact shape

Figure 5. The impact of S/D contact shape.

The contact shape also impacts the device current in our experiments. To scrutinize the impact of contact shape, we test a set of contact patterns which have the same contact area but different contact shape under the TCAD simulation conditions, meanwhile the total area of the contact is equal for all test layouts. As shown in Figure 5, as the contact length along the gate line is larger, the saturation current is increased. This is because there is less current crowding from the S/D electric field and less stress relaxation of stress liner as the longest contact length is toward in the same direction with the gate.

As we can see in Figure 2, 4, and 5, the saturation current due to the variation of S/D contact is highly dependent on the contact area, the horizontal distance from the gate line, and the contact shape along the vertical gate line. Since the saturation current is in inverse proportion to the contact resistance, we can consider the current impact of S/D contact by updating the S/D contact resistance. It implies that we get an accurate S/D contact resistance by exhibiting both the horizontal distance weighting factor and the shape weighting factor of the vertical direction.

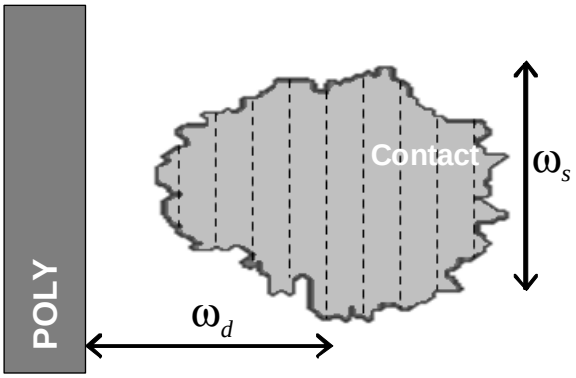


Figure 6. A compact model of S/D Contact

To estimate the current impact of contact resistance in a circuit level simulation, we propose an novel equivalent contact resistance model for various shapes of contact patterns. We first construct a set of look-up tables which include shape weighting factor, distance weighting factor for NMOS and PMOS S/D contact from the resulting Figure 2 and 5. Once the printed images of contact holes are generated, we then classify NMOS contacts and PMOS contacts. Each contact is vertically sliced by a set of equal width polygons which keeps the original contact edge as shown in Figure 6. Then, we calculate a sliced polygon area and get a shape weighting factor (ω_s) and a distance weighting factor (ω_d). The weighting factors are directly related with the saturation current. Therefore, the weighting update can be done in O(1) access time.

Given i^{th} slice of a contact, the resistance of a sliced polygon is as follows:

$$R_i = \frac{\rho}{\omega_{d,i} \cdot \omega_{s,i} \cdot A_i} \tag{3}$$

where ρ is resistivity and A_i is the area of a slice. The equivalent of a contact is computed by summing all weighted areas of sliced polygons as following equation:

$$I_{dsSat} \propto \frac{1}{R_{co}} = \sum_i \frac{1}{R_i} = \frac{1}{\rho} \cdot \sum_i (\omega_{d,i} \cdot \omega_{s,i} \cdot A_i) \tag{4}$$

Since the total contact area can be a linear function of the number of contacts [21], the total weighted area is summated for all contact holes. The total resistance is calculated by dividing the resistivity (ρ) by the total weighted area as described. By applying this compact model, we can deal with any kind of contact shapes due to the lithography variations.

5. EXPERIMENTAL RESULTS

We implemented the compact S/D contact extraction model in Tcl and Perl script language and tested with the industrial $32nm$ standard cell. The nominal contact size is $40nm$ for all standard cells. After calculating the effective S/D contact resistance, we updated the value in netlist file and measured the current and the delay using Hspice [17]. For model-based OPC and Print-image, we used Calibre-OPC/Printimage [19]. Our optical parameters are wavelength (λ) = $193nm$, numerical aperture (NA) = 1.25 immersion lithography, and quasar unpolarized illumination $\sigma = 0.9/0.7$. The thickness of photo-resist is $150nm$. For delay and current simulation, we set the nominal S/D resistance on 100Ω as defined in ITRS road-map for $32nm$ CMOS devices [22].

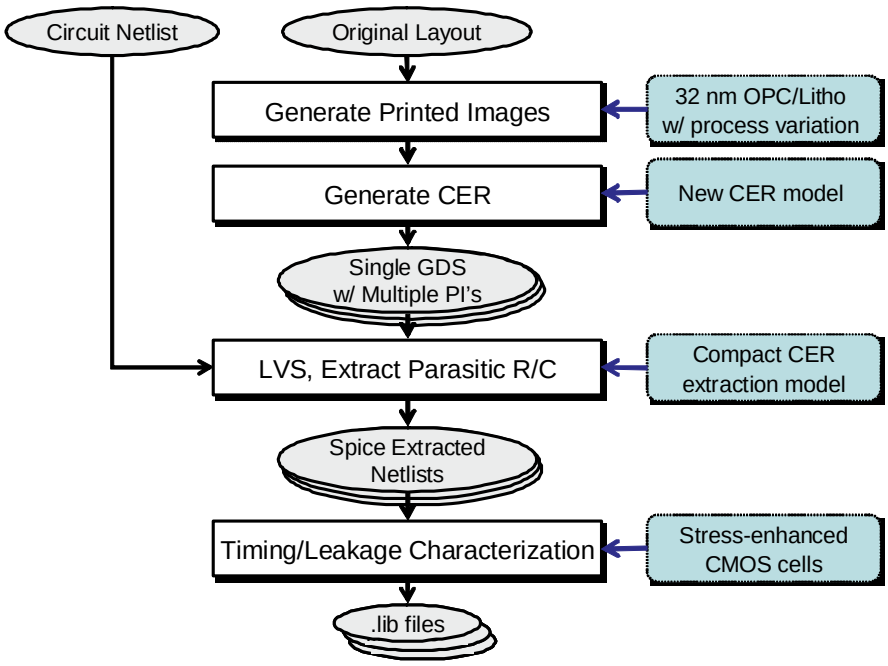


Figure 7. CER-aware cell characterization flow

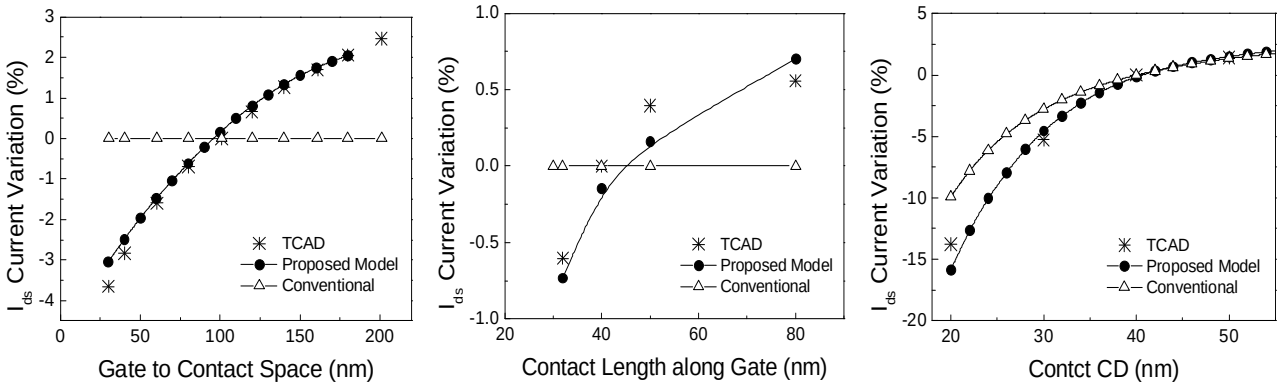
Figure 7 illustrates the overall flow of our model-based geometrical and electrical analysis toolkit. The flow is divided into three main steps:

1. **Print Image Simulation:** this step involves simulating the lithography models and generation of non-rectangular contours/shapes due to the printed image. We uses a commercial OPC and lithography simulation tools to get the print-images of the nominal condition and the process corners. After done lithography print-image simulation, rule-based etch corrections for etch proximity effects are applied to the print-images. Once we get the final print-images, we can also simulate the impact of CER. Input CER conditions are first requested, then the CER variations are added on the edge of the final print-images.

2. **Extraction with print-image:** this step extracts device dimensions considering the non-rectangular shape in the S/D contact layer due to print image. To get the parasitic resistance and capacitance parameters of a cell, we use a commercial layout extraction tool, meanwhile we back-annotate the contact resistance by our circuit level compact extraction model.

3. **Characterization for several corners:** this step characterizes the cells for delay and leakage information using the extracted parameters from previous step. We uses a commercial circuit simulation tool to get delay and power of a cell for each process corners.

The simulated print-image is written to a new layout file, which is an input file for an extraction tool. We use an industrial extraction tool to extract the devices and the parasitics in a spice netlist format. This extraction



(a) Contact displacement (b) Contact shape (c) Contact area

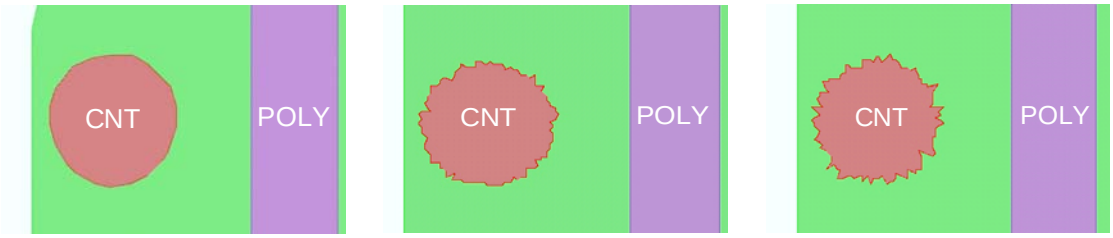
Figure 8. Validation of our compact S/D contact extraction model.

is then updated with actual contact resistance values, followed by timing and power analysis with an industrial circuit simulator. All the sequences are implemented and automated in our cell characterization flow.

We first validate our compact S/D contact model by comparing with an rigorous process/device simulation (TCAD) [18] and Hspice simulation (Conventional) [17]. Note that the conventional circuit simulation just considers the contact area variation which is directly related with the contact resistance by dividing the contact resistivity by the contact area, meanwhile it is limited to analyze the contact shape and the contact distance effect due to device stress relaxation. Figure 8 proves that our contact resistance model is well matched with TCAD results in terms of the distance from the PMOS gate (a), the contact shape (b), and the contact CD (area) of NMOS (c). The reason why our model goes with the TCAD results is that we use the contact distance and shape weighting look-up tables which are generated from accurate TCAD simulations. The result shows the great agreement with the rigorous TCAD results with the overall 0.16% current error. By directly implementing our equivalent S/D contact model into the conventional circuit model, we can handle the contact variation in fast simulation time because there is no additional simulation overhead.

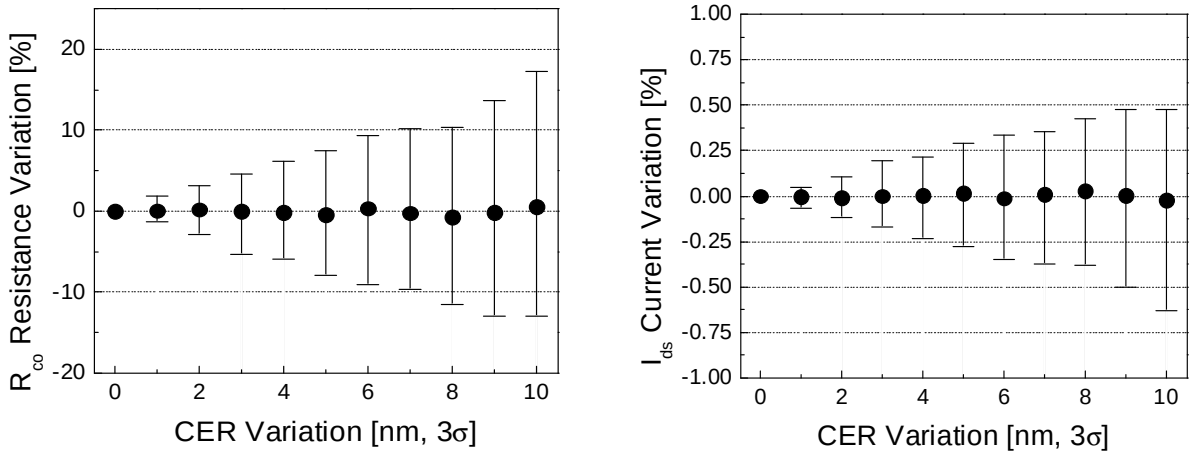
With our CER and contact extraction model, we analyzed the impact of CER on the S/D contact resistance and the saturation current. We first ran the contact OPC and print-image simulation with the best optical condition. Then we swept CER on the contact printed images 3σ from $0nm$ to $10nm$ as shown in Figure 9. To understand the impact of CER, the only input variable is the rms value of CER, thus we fixed all other lithography process variables, e.g., dosage, focus and mask bias. We generated more than one thousand CER pattern for a particular rms value of CER so that the results are shown as a distribution.

We first investigated the S/D contact resistance variation with the amount of CER, then the device saturation current variation in an industrial $32nm$ Inverter standard cell where the nominal contact CD is $40nm$. It assumes that CER is generated on top of circular shape of contacts. Figure 10 shows the impact of CER on the contact



(a) No CER (b) CER 3σ = 4nm (c) CER 3σ = 8nm

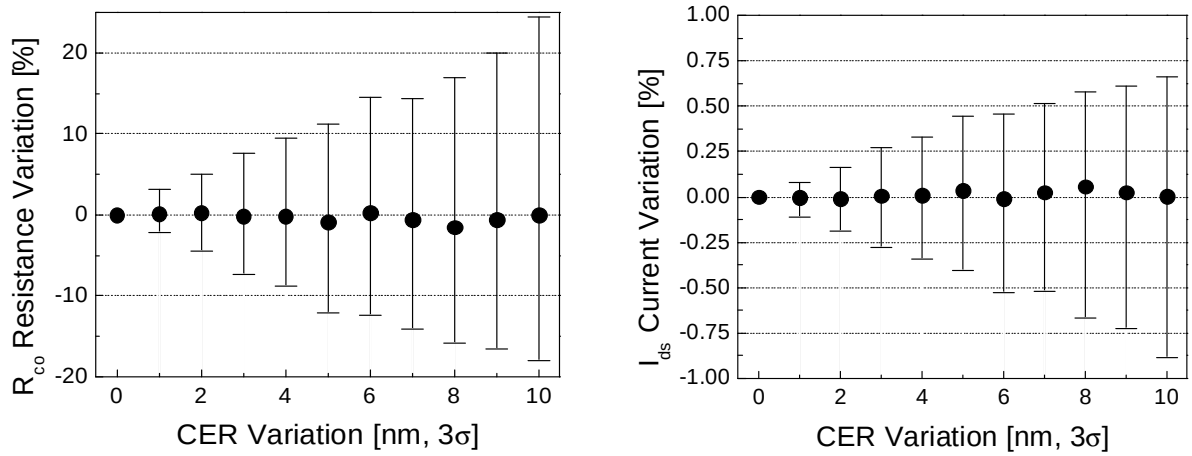
Figure 9. CER simulation



(a) Variation of the S/D Contact resistance

(b) Variation of the device saturation current

Figure 10. The impact of CER on the contact resistance and the saturation current when the area variation of the S/D contact is the only factor of the contact model in a conventional NMOS cell.



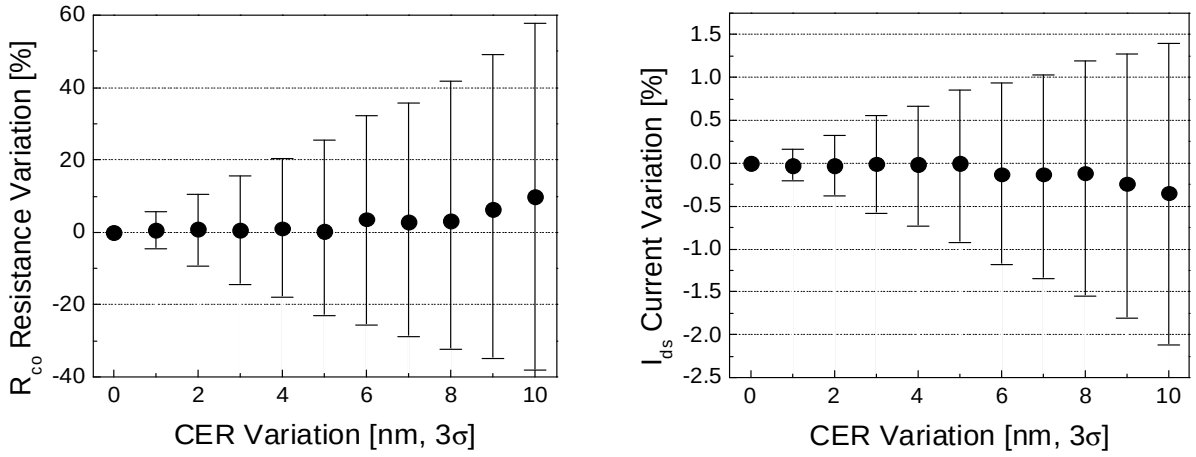
(a) Variation of the S/D Contact resistance

(b) Variation of the device saturation current

Figure 11. The impact of CER on the contact resistance and the saturation current when the position, shape and area weighting factors are considered in a stress enhanced NMOS cell.

resistance and the saturation current in a conventional NMOS devices which does not use stress liner. Since we assume that the position and shape variations of the contact do not affect the variation of the contact resistance in this case, the area variation of the S/D contact is the only factor of the contact model. The black circled dot represents the average of the variation, and the small rectangular bar shows the upper and lower bound of the variation in Figure 10. As shown in the results, the deviation between the upper bound and the lower bound is increased as the CER increases while the average values are no significant difference. The result reveals that the variation of the S/D contact resistance and the saturation current are as much as 17.3% and 0.64%, respectively where the rms CER value is $10nm$ from its nominal contact edge.

In the similar fashion, as shown in Figure 11 we analyzed the S/D contact resistance and the device saturation current variation with our rigorous S/D contact extraction model in a stress enhanced NMOS devices which has a tensile stress liner. It also assumes that CER is generated on top of circular shape of contacts. The contact position and shape weighting factors are also considered in this case to get the more accurate contact resistance value. Even though the geometrical center of a contact is not changed in the standard cell, the result reveals that



(a) Variation of the S/D Contact resistance

(b) Variation of the device saturation current

Figure 12. The impact of CER on the contact resistance and the saturation current when CER causes the change of the S/D contact area.

the variation of the S/D contact resistance and the saturation current are up to 24.5% and 0.90%, respectively where the rms CER value is $10nm$. When compared with Figure 10, Figure 11 shows as much as 7% and 0.3% increase in the S/D contact resistance and the saturation current, respectively. This is because the higher CER makes a contact pattern easy to be distorted which causes the change of the contact shape, area and even displacement from the center. Due to the small process window (tolerance) of contact patterns, the $10nm$ of CER could be happened in an sub-$32nm$ lithography process, which means that over 24% change of the S/D contact resistance could be occurred.

Figure 12 shows the impact of CER on the contact resistance and the saturation current when CER causes the change of the S/D contact area according to the rms roughness of CER. As mentioned in Introduction, when the 3 σ roughness of CER is $4nm$, the S/D contact area variation is as much as 10% in our $32nm$ contact manufacturing. This is because CER affects on the contact shape which causes a highly change of S/D contact area. The result presents that the variation of the S/D contact resistance and the saturation current are up to 57.8% and 2.12%, respectively where the rms CER value is $10nm$. Meanwhile the average value of the resistance is slightly increased, and the trend of the saturation current is slightly decreasd. When compared with the results of Figure 11, the resistance and the saturation current of S/D contact are increased more than double. If the systematic process variation of which impact is more than random CER is applied to the contact patterning, the parametric variation should be increased.

6. CONCLUSION

We have proposed a CER model and a novel S/D contact extraction model to electrically analyze S/D contact having CER. Our contact extraction model is based on the contact shape and displacement weighting factor and is well matched with a rigorous TCAD simulation. Experimental results with a industrial cell library show that the portion of the random CER in parametric variation is considerable in sub-$32nm$ standard cell. We believe a flow that is capable of characterizing CER variability will demonstrate significant advantages in terms of understanding the impact of CER and improving systematic yield and parametric yield as a result of reducing design-to-manufacturing mis-correlations.

7. ACKNOWLEDGEMENTS

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