Exploration of VLSI CAD Researches for Early Design Rule Evaluation

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Abstract -- Design rule has been a primary metric to link design and technology, and is likely to be considered as IC manufacturer's role for the generation due to the empirical and unsystematic in nature. Disruptive and radical changes in terms of layout style, lithography and device in the next decade require the design rule evaluation in early development stage. In this paper, we explore VLSI CAD researches for early and systematic evaluation of design rule, which will be a key technique for enhancing the competitiveness in IC market.

I. Introduction

For the generation of design rule (DR), there are three primary costs: process, device and layout area. All DR challenges are induced by the fabless and manufacturer's requirements to follow Moore's law. Figure 1 shows a simple schematic to explain the challenges of design rule generation. Process cost limit (PCL) represents the cost to build device structure and is determined by lithography and etching costs. The PCL is typically a lower bound in DR size axis. Device cost limit (DCL) is the cost to satisfy device performance target. Area cost limit (ACL) depends on the cost for Logic/SRAM cell dimension and determines the upper bound of DR size. Design rule is determined by the three common windows. As the scaling goes into nanometer regime, the common window gets smaller. Several efforts to put DRs into the common window include double patterning lithography (DPL) for process cost [1-2], strain-driven performance boosting for device cost, local interconnect and regular layout style for area cost [3].

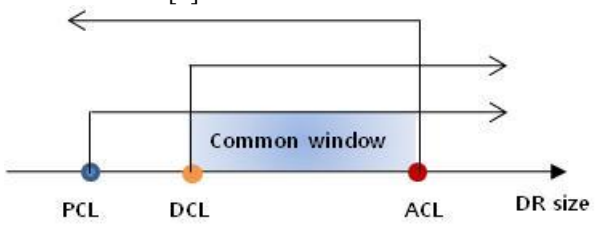


Figure 1. Simple schematic of three primary costs.

In this paper, we explore the VLSI CAD researches to develop design rule and introduce frameworks to assess the design rule in terms of process, device and area metrics. Research directions will be discussed with examples in following sections.

II. VLSI CAD Researches

A. *Process (lithography) evaluation*

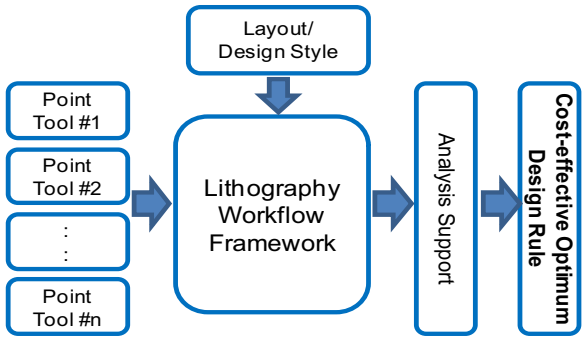
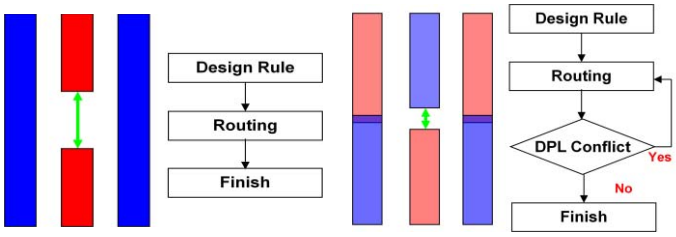


Figure 2. Lithography workflow framework.

Due to the growing number of tool, material and process changes required at each successive technology generation, exploration of optimum design rules for a technology node is an increasingly complicated and time consuming activity. Many good modeling tools are available for process and layout predictions. However, generally these modeling tools are designed to work as a point tool for individual optimization of a process or sub-process, they are not designed to connect to a range of other point tools. For an optimization activity as complex as design rule exploration, better integrated flow and analysis methods are required in order to reduce the high time and effort needed to be successful with point tools. We propose the lithography workflow framework in Figure 2.



(a) Relaxed design rule (b) Aggressive design rule

Figure 3. DPL aware design rule.

DPL is the only choice for sub-20nm patterning, which causes a new interaction between router and design rule. There are two approaches to enhance decomposability for the metal DPL. The first approach is to enforce router decomposable by using relaxed design rule. We can avoid patterns that generate native conflicts by relaxed Tip-Tip-Side rule as shown in Figure 3 (a), which can make sure to remove indecomposable odd-cycle patterns [4]. However, since relaxed DR increases overall chip area, we need to be careful to define DR for DPL friendly layout. More aggressively, we can use non-relaxed

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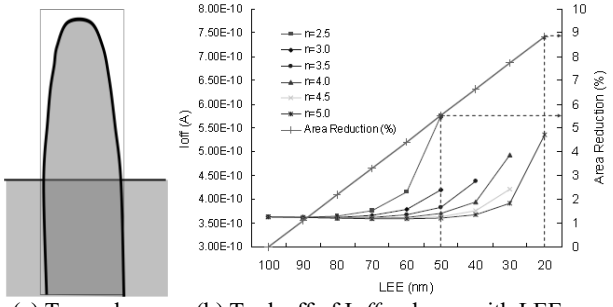
rule as shown in Figure 3 (b). In the case, decomposability must be guaranteed by smart routing algorithm. If we can remove native conflicts during routing, the role of DR for DPL friendly layout will be ignorable. We show router requirements between relaxed and aggressive design rule. We thus believe that these two knobs have to be co-optimized for DPL friendly layout within reasonable routing time.

B. Device performance

Device cost decides the parametric yield and is the leftmost bound of the common window. However, it seems not easy to consider the device performance due to the device stability in early stage. So, research for prediction modeling is essential for the co-optimization of device and process.

Predictive compact model (PCM) is the approximated device model. PCM requires capturing only dominant non-ideal behaviors such as Drain Induced Barrier Lowering (DIBL), body effect, and non-ideal sub-threshold slopes. We observe that the approximated model is better than providing accurate model in terms of timing and power estimation when we compared with an equivalent full-featured device model. The main difficulty of generating PCM is to build accurate model with limited experiments because we need rapid model generation to estimate the cell or block level performance for design and process co-optimization. Therefore, PCM is only required to support limited geometry scales and PVT corners for the purpose of process assessment.

For more accurate TCAD based PCM generation, we need to capture I*off* and I*on* change according to lithography shape [5]. Figure 4 shows the tradeoff curve of I*off* and area according to line-end extension (LEE) rule. We observe that the traditional line-end extension design rule can be reduced further without affecting electrical characteristics of the circuits. Our next direction is to provide rules of thumb by which photo and design engineers can co-optimize electrically safe, phot-lithographically robust yet cost-effective, area-conserving line-end design rules.



(a) Taper shape (b) Tradeoff of I*off* and area with LEE

Figure 4. DR optimization with line-end TCAD modeling.

C. Area estimation

Area impact according to DR changes is sensitive to not only design and process, but also marketing due to the direct impact on a chip-price competition. Thus, it is very valuable to develop an area estimator of standard cell. The estimator must allow quick evaluation with DR updating.

For standard cell-level estimation, a few design rules are related to the area. For example, poly-to-poly, poly-to-dummy, poly-to-active spacings, and NMOS/PMOS width and poly line-end extension determine the standard cell dimension. Thus, area assessment should be done within a few hours even with several hundred of standard cells [6]. Figure 5 show a comparison of layout dimension between actual and virtual libraries. The experiment result shows the dimension accuracy error <4% and runtime <10 hours with over 500 number of standard cell.

For chip-level area estimation, the track congestion comparison, i.e., ratio between available routing tracks and occupied routing tracks can be used instead of DR. However, in the DPL regime, the estimator has to assess the actual DRs, for example, tip-to-tip spacing DR for LELE and trim width and spacing DRs for SADP [4].

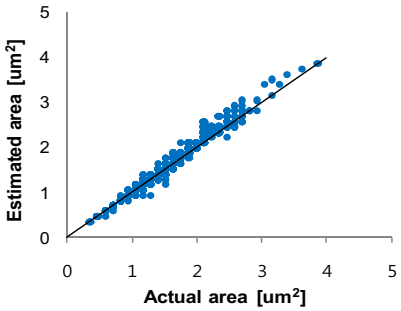


Figure 5. Accuracy of area estimator in standard cell.

III. Conclusions and Future Work

We investigate VLSI CAD researches for design rule evaluation. Since the evaluation is performed in early development stage, the key research directions include: (1) accurate model building with simulations and a few experiments, (2) runtime for assessment of many DRs and (3) framework for co-evaluation of process, device and area.

Acknowledgments

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