# Design for Manufacturability and Reliability for TSV-based 3D ICs

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***Abstract*—The 3D IC integration using through-silicon-vias (TSV) has gained tremendous momentum recently for industry adoption. However, as TSV involves disruptive manufacturing technologies, new modeling and design techniques need to be developed for 3D IC manufacturability and reliability. In particular, TSVs in 3D IC may cause significant thermal mechanical stress, which not only results in systematic mobility/performance variations, but also leads to mechanical reliability concerns such as interfacial cracking. Meanwhile, the huge dimensional gaps between TSV, on-chip wires, and bonding/packaging all lead to new electromigration concerns. Thus full-chip/package modeling and physical design tools need to be developed to achieve more reliable 3D IC integration. In this paper, we will discuss some key design for manufacturability and reliability challenges and possible solutions for TSV-based 3D IC integration, as well as future research directions.**

## I. Introduction

A major focus of the semiconductor industry in the last 4-5 decades has been to miniaturize ICs by advanced lithography patterning technology, which is now around 22nm node. While ITRS still predicts further CMOS scaling, e.g., to around 7nm node by the year of 2020 [1], such scaling will reach fundamental physical limit, or even before that happens, the economy of scaling will require other means for "more Moore" and "more than Moore" integration. Due to the increasing power, performance, and financial bottlenecks beyond 32-22nm, industry began to look for alternative solutions. This has led to the active research, development, and deployment of thinned and stacked 3D ICs, initially by wire-bond, later by flip-chip, and recently by Through-Silicon-Via (TSV). TSV provides the possibility of arranging digital and analog functional blocks across multiple dies at a very fine level of granularity. This results in a decrease in the overall wire length, which naturally translates into less wire delay and less power. Advances in 3D integration and packaging are undoubtedly gaining momentum and have become of critical interest to the semiconductor industry.

Compared with other layout objects on a chip, TSVs are quite large in size, e.g., a few times larger than minimum size NAND2, thus they become significant layout obstacles: they occupy bulk and device layers in case of via-first TSV, or occupy the entire die stack in case of via-last TSV. During 3D IC manufacturing, different coefficients of thermal expansion (CTE) mismatch between copper TSV and silicon can cause thermal-induced stresses, as shown in Fig. 1. For TSV manufacturing, tungsten (W), poly-silicon, and copper(Cu) have all been considered as fill materials of TSVs. Since copper has low resistivity, it is widely used material for TSV fill. However, copper CTE differs from silicon CTE which can be a source of silicon strain. CTE of copper is $17\times10^{-6}K^{-1}$ at $20°C$, while CTE of silicon is $3\times10^{-6}K^{-1}$ at $20°C$ [2]. The CTE mismatch between copper and silicon causes inevitable stress on silicon. Because the copper electroplating and annealing temperature is higher than chip operating temperature, tensile stress appears on silicon [3], [4] after cooling down to room temperature.

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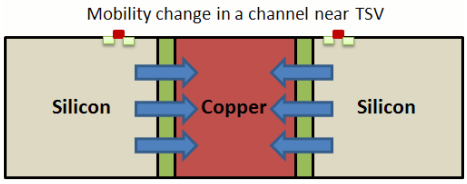


Fig. 1. Thermal mechanical stress around a TSV [5].

The thermal mechanical stress due to TSV will cause the nearby silicon lattice structure deformation, which will change the mobility of PMOS and NMOS. Interestingly, the tensile stress cause different mobility changes for PMOS and NMOS, thus stress-induced electrical variations need to be considered. TSVs not only cause mobility/performance variations, but also lead to mechanical reliability concerns such as interfacial cracking. Meanwhile, the huge dimensional gaps between TSV, on-chip wires, and bonding all lead to new electromigration (EM) concerns. There have been limited studies on TSV simulations, mostly using finite element analysis (FEA). While FEA methods can perform detailed analysis of a single TSV, they are simply too expensive for full-chip scale which may have thousands of TSVs. Thus full-chip modeling and physical design tools need to be developed to achieve reliable and robust 3D ICs. In this paper, we will discuss several key design for manufacturability and reliability issues for TSV-based 3D ICs.

The rest of this paper is organized as follows. In Section II, full-chip TSV-induced thermal mechanical stress modeling will be shown, using a first-order linear superposition method. Then in Section III, the electrical performance variations of TSVs will be investigated using the full-chip modeling with its application in layout optimizations. In Section IV, new electromigration issues with TSV will be shown, which heavily depend on the thermal mechanical stress. So is the case for interfacial cracking, as shown in Section V. Other manufacturability and reliability issues will be discussed in Section VI, followed by conclusion in Section VII.

## II. Full-chip Thermal Mechanical Stress Analysis

Most previous works on thermo-mechanical stress induced by CTE mismatch between TSV and substrate materials have been limited to a single TSV in isolation or up to a small number of TSVs [7]–[10]. This is because FEA simulations for multiple TSVs require huge computing resources and time. Thus it is not suitable for full-chip analysis. To overcome this limitation, full-chip thermo-mechanical stress analysis flow based on the principle of linear superposition of stress tensors from individual TSVs was proposed [6], [11].

The linear superposition principle states that stresses and displacements of a linear elastic body induced by a number of forces

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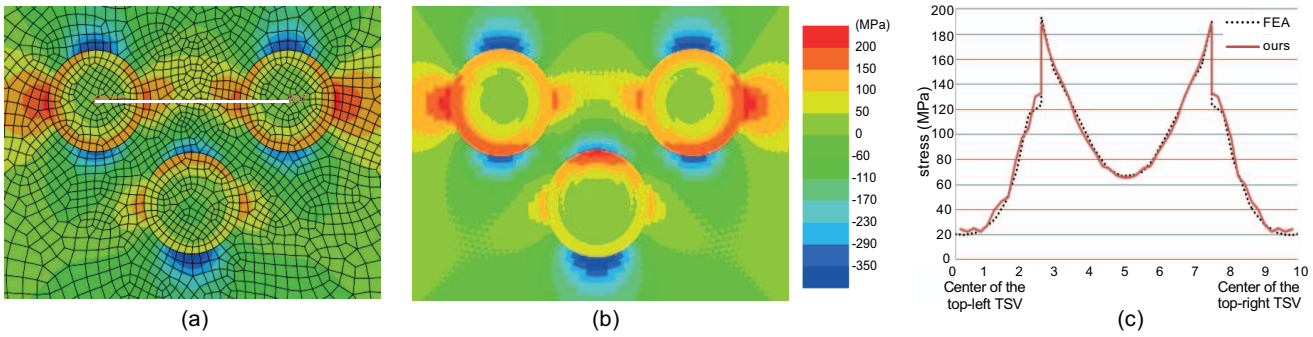



Fig. 2. Sample stress comparison between FEA simulation and linear superposition method. [6] (a) FEA result ($\sigma_{xx}$). (b) ours ($\sigma_{xx}$). (c) FEA vs. ours ($\sigma_{xx}$) along the white line in (a).

acting simultaneously are the sum of the effects of the forces applied separately. Assuming all the materials in TSV structure are linear elastic, we can compute stress at a point by simply adding the individual stress tensors from each TSV at that point.

First, based on the observation that the stress field of a single TSV in isolation is radially symmetrical due to the cylindrical shape of a TSV, stress distribution around a TSV can be obtained from a set of stress tensors along an arbitrary radial line from the center of a TSV in a cylindrical coordinate system. To evaluate a stress tensor at a point affected by multiple TSVs, a conversion of a stress tensor to a Cartesian coordinate system will be performed. Then, we can compute the stress tensor at any point of interest by adding up stress tensors from TSVs affecting this point.

Let stress tensor in Cartesian and cylindrical coordinate is $S_{xyz}$ and $S_{r\theta z}$, respectively.

$$S_{xyz} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix}, S_{r\theta z} = \begin{bmatrix} \sigma_{rr} & \sigma_{r\theta} & \sigma_{rz} \\ \sigma_{\theta r} & \sigma_{\theta\theta} & \sigma_{\theta z} \\ \sigma_{zr} & \sigma_{z\theta} & \sigma_{zz} \end{bmatrix}$$

The transform matrix Q is the form:

$$Q = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

where $\theta$ is the angle between the x-axis and a line from the TSV center to the simulation point. A stress tensor in a cylindrical coordinate system can be converted to a Cartesian coordinate system using conversion matrices: $S_{xyz} = QS_{r\theta z}Q^T$.

The basic algorithm for generating stress map is illustrated in algorithm 1. We first find the stress influence zone for each TSV. Essentially, TSV-induced stress impact will be negligible at any point which is very far away. Then, we associate the points in the influence zone with the affecting TSV. Next, for each simulation point under consideration, we look up the stress tensor from the TSV found in the association step, and use the coordinate conversion matrices to obtain stress tensors in the Cartesian coordinate system. We visit every individual TSV affecting this simulation point and add up their stress contributions. The stress tensor for each individual TSV is computed from very detailed FEA simulations and then stored in a look-up-table. The complexity of this algorithm is $O(n)$, where $n$ is number of simulation points.

The proposed full-chip thermo-mechanical stress has been validated against FEA simulations for multiple TSV scenarios. We observed that the error between the linear superposition method and FEA simulations is less than 5%, with realistic TSV sizes and pitches (e.g., TSV pitch of $7\mu m$, with TSV diameter of $5\mu m$). As we further decrease TSV pitch, due to strong TSV-to-TSV interaction,

**input** : TSV list $T$, stress library, thermal map (optional)
**output**: stress map
**for** *each TSV $t$ in $T$* **do**
  $c \longleftarrow$ center of $t$
  $r \longleftarrow$ FindStressInfluenceZone($c$)
  **for** *each point $r'$ in $r$* **do**
    $r'.TSV \longleftarrow t$
  **end**
**end**
**for** *each simulation point $p$* **do**
  **if** $p.TSV \neq \emptyset$ **then**
    **for** *each $t \in p.TSV$* **do**
      $d \longleftarrow distance(t, p)$
      $S_{cyl} \longleftarrow$ FindStressTensor($d, temperature$)
      $\theta \longleftarrow$ FindAngle($line\ tp, x\ axis$)
      $Q \longleftarrow$ SetConversionMatrix($\theta$)
      $S_{Cart} \longleftarrow QS_{cyl}Q^T$
      $p.S_{Cart} \longleftarrow p.S_{Cart} + S_{Cart}$
    **end**
  **end**
**end**

**Algorithm 1:** Full Chip Stress Analysis Flow [6]

the error starts to increase. However, since a typical copper TSV pitch achievable in the current process is around $10\mu m$, with $5\mu m$ diameter TSV [12], this linear superposition method is valid in practice. Figure 2 shows a test case which contains three TSVs, and it clearly shows that the linear superposition method matches well with the detailed FEA simulations.

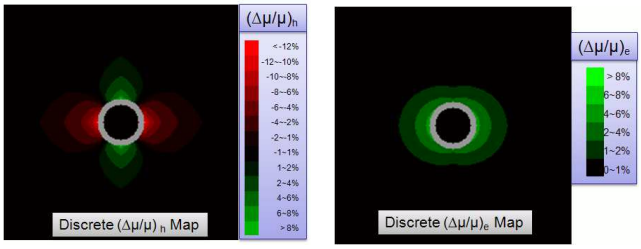
However, there are still challenges to overcome. First, our model is based on one silicon substrate die containing TSVs. However, thermo-mechanical stress distribution around TSV can be highly affected by package components [13]. Therefore, this impact of package components on the stress should be carefully evaluated. Also, the error between linear superposition and FEA tends to increase when TSV pitch becomes smaller. Thus, new full-chip and package level modeling for the thermal mechanical stress needs to be developed. It is also important to get the measurement data to validate different liner material, landing pad sizes, package, and so on.

## III. Stress-aware Performance Modeling and Optimization

The tensile stress on silicon can change mobility of carriers. In [14], Thompson et al. reported that longitudinal tensile stress reduces hole mobility whereas transverse tensile stress increases the

mobility. Yang et al. suggested in [15] that TSV stress induced by CTE mismatch may cause timing violation if cells on a critical path are placed near TSVs. If PMOS is on a critical path, it can cause unexpected setup time violation which is not detected with the timing analysis flow. They proposed a design flow to analyze timing variation by TSV induced stress.

To take TSV-induced stress into account for stress-aware 3D static timing analysis (SA-3D-STA), an analytical model of TSV stress-induced carrier mobility variation was proposed in [15]. Carrier mobility change depends not only on applied stress, but also on orientation between the stress and the PMOS/NMOS transistor channel. Fig. 3(a) shows a contour map for hole mobility variation. In the contour, hole mobility decreases in a horizontal direction, but it increases in a vertical region. No hole mobility change is observed in $45^\circ$ direction. Contour map for electron mobility variation is presented in Fig. 3(b). Horizontal direction has more mobility enhancement zone. The effect from multiple TSVs can be combined by using linear superposition.




(a) Contour map for hole mobility variation

(b) Contour map for electron mobility variation

Fig. 3. Mobility contour map for a TSV [15].

Even though the layout of a cell is fixed, its timing characteristic can vary based on TSV stress-induced carrier mobility variation. The SA-3D-STA framework in [15] renames cells in Verilog netlist to reflect their carrier mobility variation. For example, Inverter `I2` in Fig. 4, `INVX1_N8_P8` is `INVX1` with negative 8% hole mobility change and positive 8% electron mobility change. Cells with different mobility corners are characterized to make carrier-mobility variation-aware library. In the framework, a Verilog netlist and a parasitic extraction file (SPEF) for each die is prepared. A top level Verilog netlist instantiates the dies, and connects them using wires, which correspond to TSVs. Finally, with a top level SPEF file for the TSVs, PrimeTime can provide the SA-3D-STA results.

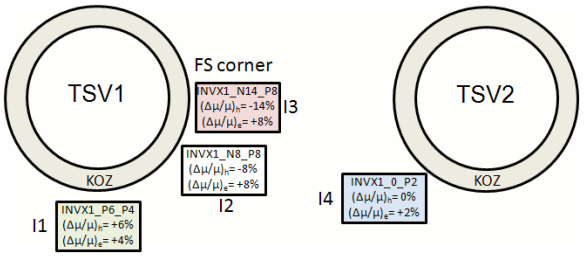



Fig. 4. Timing corner determination according to mobility variation [15].

With TSV stress-induced mobility variation modeling and SA-3D-STA framework, [15] demonstrated that stress-induced mobility can actually be exploited to improve timing on critical cells. Stress-aware layout perturbation could reduce cell delay by up to 14.0 % and critical path delay by 6.5 % in their test cases.

Due to uncertainty of the stress-induced variations and other possible impacts on reliability, the keep-out zone (KOZ) is proposed, i.e., no logic cells are allowed to be placed within certain area surrounding a TSV so that they are not influenced by the TSV-induced stress. To determine the size of KOZ in [16], Okoro et al. analyzed the magnitude of stress caused by TSVs. KOZ is usually large because it is defined such that stress outside it is under preset tolerance (negligible). In real designs, however, the presence of hundreds/thousands of TSVs will have tremendous impact on 3D IC layout. In [17], Athikulwongse et al. demonstrated that large KOZ will increase the die size, as illustrated in Fig. 5.

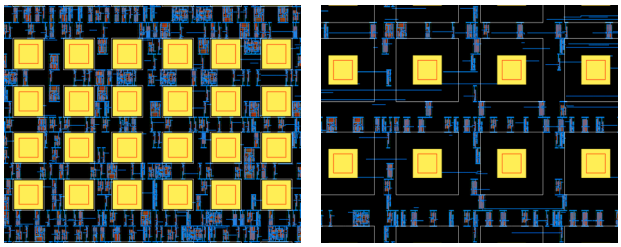


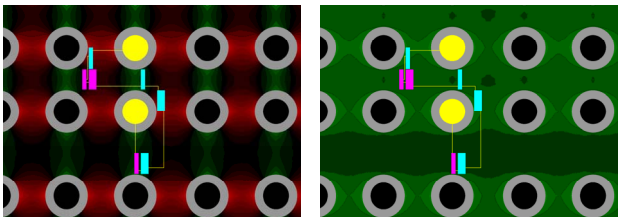
Fig. 5. Layouts with small versus large KOZ around TSVs [17]. TSV landing pads are large yellow squares.

To reduce KOZ without adverse electrical effect, placers must consider the effect of TSV-induced stress on carrier mobility variation. The first TSV-induced stress-driven force-directed 3D global placement algorithm was proposed in [17] to exploit the systematic hole and electron mobility variations caused by TSV-induced stress. Carrier mobility-based forces are introduced to a 3D force-directed quadratic placer such that logic cells on critical paths are placed in the position where the carrier mobility inside their PMOS/NMOS is not degraded or even enhanced by TSV-induced stress. Essentially we can take advantage of the systematic stress-induced mobility variations through intelligent timing-timing placement. Therefore, there is indeed no need to enforce a large KOZ for timing/performance reason, as long as we can model the stress-induced variations efficiently and accurately. We only need to set the KOZ for basic reliability requirement.

A few stress-driven placement snapshots are shown in Fig. 6. In the figures, gray band surrounding TSVs is KOZ. Logic cells in magenta are hole mobility critical cells. Their timing arcs are rising on the critical paths. They are positioned (if possible) in green area of Fig. 6(a) where they receive hole mobility enhancement, or, at least out of bright red area where they experience severe hole mobility degradation. On the other hand, logic cells in sky blue color are electron mobility critical cells. Their timing arcs are falling on the critical paths. They are positioned (if possible) in bright green area of Fig. 6(b) where they receive higher electron mobility enhancement.

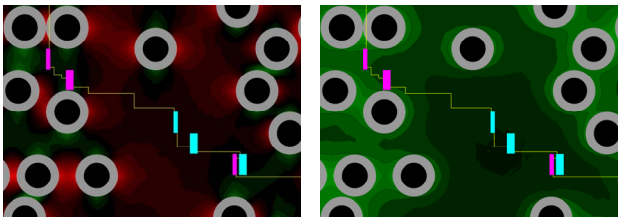
Besides path delay, carrier mobility variation caused by TSV-induced stress can affect clock buffer, resulting in unexpected skew which degrades overall chip performance. In [5], Yang et. al proposed a clock tree design methodology that minimizes clock period variation by assigning optimal tier or die (z-location) for clock buffers with an Integer Linear Programming (ILP) formulation, which prevents unwanted skew induced by the stress. It also takes advantage of the uncorrelated variations at different dies. The clock buffer tier assignment reduces clock period variation by up to 34.2%, and most of stress-induced skew can be removed by stress-aware clock tree synthesis (CTS). Overall, the entire clock period can be shortened by up to 5.7% with this new 3D-IC aware CTS algorithm.

The works in [5] and [17] considered only carrier mobility variation caused by TSV-induced stress. However, other stress sources inside ICs were not included, such as shallow trench isolation (STI), SiGe stained silicon, and so on. Placement perturbation techniques were



(a) With regular TSV position on hole mobility variation surface

(b) With regular TSV position on electron mobility variation surface



(c) With irregular TSV position on hole mobility variation surface

(d) With irregular TSV position on electron mobility variation surface

Fig. 6. Zoom-up snapshots of stress-driven placement results [17].

proposed to use STI-induced stress [18] and strained silicon [19] for performance optimization. These stress sources may interact with each other, resulting in changes in total mobility variation. Therefore, the effects of all of them should be considered together.

## IV. Electromigration Analysis and Layout Optimization

In classical electromigration (EM) studies, Black [20] proposed an empirical equation to relate the mean-time-to-failure (MTTF) of metal interconnects to current density and temperature. However, a lot of experimental works and modeling studies have shown that Black's equation is not accurate enough to predict the failure in metal interconnects [21].

EM failure in interconnects may be caused by several other interacting forces as well. These forces include current density, temperature gradient, mechanical-stress gradient, and atom concentration gradient. The migration of atoms caused by each of these forces can be categorized as follows [21]: (1) current-induced migration (CM) caused by moving electrons of current, (2) stress-induced migration (SM) caused by thermo-mechanical stress gradient, (3) temperature-induced migration (TM) caused by temperature gradient, and (4) atomic migration (AM) caused by atomic concentration gradient. The variation of atomic concentration in a metal structure can be represented by the following equations:

$$\frac{\partial c}{\partial t} + \nabla \cdot \Gamma = 0 \tag{1}$$

$$\Gamma = -D\nabla c + \frac{Dcje\rho Z}{kT} + \frac{Dc\Omega}{kT} \cdot (\nabla(\sigma_m)) + \frac{DcQ^*}{kT} \cdot \frac{\nabla(T)}{T} \tag{2}$$

where $D = Do\ exp(-E_a/kT)$. The variables and the equations are discussed in greater details in [21].

The recent paper [22] examined electromigration challenges for a single TSV structure. It considered the stress generated by TSV when modeling the electromigration effect. The paper also discussed about the regions that are most likely to fail within the TSV. A more recent work [23] looked at the TSV structure and the stress effects in greater detail. The Figure 7 shows how atomic concentration varies along a TSV structure. The paper considered a 3-dimensional model of TSV when considering the impact of TSV stress. It also considered the effect of nearby materials such as interlayer dielectric (ILD), silicon

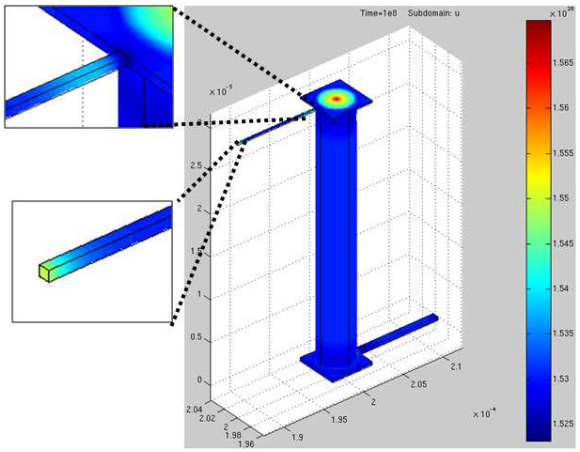


Fig. 7. Variation of atomic concentration along a given TSV [23].

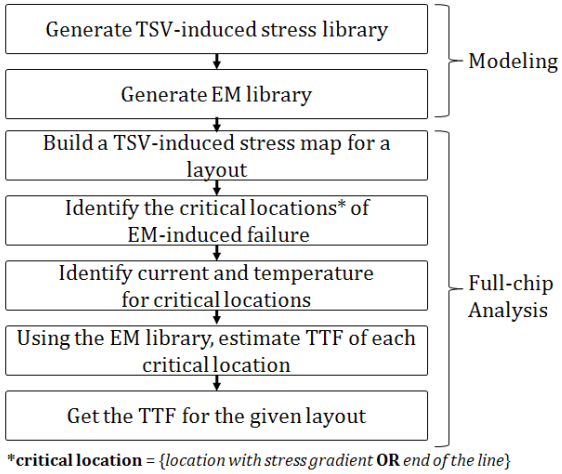



Fig. 8. Generating libraries and estimate the EM time-to-failure for a full-chip layout based on the libraries [24].

dioxide and benzocyclobuten (BCB). Impact of various parameters like the size of the TSV and its landing pad were also investigated. It showed that the stress generated by the TSV not only impacts the TSV structure itself, but can also impact the electromigration reliability of the nearby metal wires. Another paper [24] considered the impact of TSV stress on the electromigration reliability of BEOL (back-end-of-line) wires in detail. They proposed a fast full-chip electromigration reliability analysis method for BEOL wires in stacked 3D ICs. They showed how stress and electromigration modeling can be done together to build more accurate models and various libraries. These libraries can then be used effectively to perform fast electromigration analysis of metal wires in 3D ICs. Fig. 8, shows the overall flow to perform electromigration analysis for full-chip scale.

These preliminary studies showed that mechanical stress can have a significant impact on the electromigration reliability of 3D ICs. However, a lot of questions and challenges still remain and need to addressed. The works in [22] and [23] looked into the electromigration reliability of the individual TSV structure in detail. However, they do not consider the impact of nearby TSVs. Multiple TSVs in close proximity may lead to more serious EM issues. In addition, TSVs can be fabricated using different methods which can be largely classified as via-first, via-last and via-middle TSVs [25]. Thus, the impact of

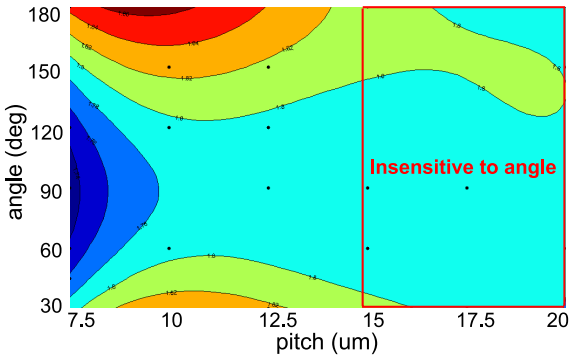



Fig. 9. ERR contour map of pitch and angle [27].

different fabrication methods on electromigration analysis needs to be further investigated. In the previous works, the EM impact of a single TSV in a single die is considered. However, stress profile can change depending on multiple die stacking and packaging components. All these issues need to be addressed to better understand the 3D-IC and package electromigration.

## V. Crack Analysis and Layout Impacts

It is widely known that most of the mechanical reliability failures occur at the interface between different materials. Since the highest thermo-mechanical stress builds up at TSV/dielectric liner interface, there is a higher chance of crack initiation and growth at this interface. Most previous works focused on modeling the thermo-mechanical stress and reliability (crack) of a single TSV in isolation [8], [9], [26]. These simulations are performed using finite element analysis (FEA) method which is computationally expensive or infeasible for full-chip analysis. To overcome this limitation, a full-chip TSV interfacial crack analysis flow based on design of experiments (DOE) and response surface method (RSM) was proposed in [27].

TSV interfacial crack initiates around the circumference of the TSV near the wafer surface and grows vertically downward [8], [9]. This TSV interfacial crack can cause not only mechanical reliability problems, but possible functional failure or performance degradation due to increase in both TSV bulk and contact resistance. Energy release rate (ERR) is a reliability metric, which is defined as the energy dissipated during fracture, i.e., crack, per newly created fracture surface area. If ERR is greater than a threshold value (debonding energy), then crack grows further unstably. This debonding energy is material and fabrication process specific. For example, the debonding energy of Cu/$SiO_2$ interface ranges from 0.7 to 10 $J/m^2$ [26].

In [27], impacts of TSV placement style, keep-out-zone (KOZ) size, and liner material/thickness on ERR were discussed. Before discussing detailed crack modeling results, we introduce two terminologies: (1) **Victim TSV**: TSV with an interfacial crack. (2) **Aggressor TSV**: TSV located nearby a victim TSV and affecting crack growth of the victim TSV.

[27] used two aggressor TSVs as an example, and performed FEA simulations on design points generated by a DOE process. Fig. 9 shows an ERR contour map (RSM) of a victim TSV for different pitches and angles. We observe high angular dependency on ERR up to 15 $\mu m$ pitch. However, as the pitch exceeds 15 $\mu m$, impact of angle is almost negligible. We further investigate the relative importance between pitch and angle on ERR up to eight aggressors. We find that angular dependency is almost not noticeable beyond 10 $\mu m$ pitch, and the number of aggressor TSVs as well as TSV pitch mostly determine the ERR value of the victim TSV.

In general, TSV placement style is largely divided into two categories, i.e., regular TSV placement and irregular TSV placement. The two important factors that determine ERR of a victim TSV in case of regular TSV placement style is TSV pitch and the victim TSV location inside TSV blocks due to its regularity. On the other hand, there are too many scenarios for irregular TSV placement results; hence it is impossible to enumerate and model all these cases. Fortunately, we observe that the gradient of ERR along TSV pitch is not steep and angular dependency on ERR is only dominant for small TSV pitches. To reduce the number of input factors for DOE and RSM, we use distance binning by grouping TSVs within a similar distance (5 $\mu m$ range) and considering angular dependency within 10 $\mu m$ distance from victim TSV. In addition, we only consider aggressor TSVs within 30 $\mu m$ from victim TSV (crack influence zone), since beyond this distance the impact of aggressor TSV is negligible.

Based on the ERR models and full-chip analysis, we identify that TSV interfacial crack is affected by TSV placement style, KOZ size, and TSV surrounding structures such as liner and landing pad. First, irregular TSV placement suffers from higher ERR and larger ERR variation compared with regular TSV placement; hence it is hard to control TSV interfacial crack problems across a chip. Thus, it is recommended to use array type TSV blocks wherever possible for regular TSV placement and block-level design to benefit from ERR reduction of the highest destructive stress interference. Meanwhile, TSV pitch inside TSV blocks should be carefully determined by considering both mechanical and electrical issues. In addition, larger KOZ relieves TSV interfacial crack due to increased spacing among TSVs and decreased number of aggressors affecting victim TSV inside crack influence zone. However, since it comes with larger footprint area, a careful design of KOZ is required. Liner material and thickness are also key design knobs to alleviate TSV interfacial crack problem by reducing stress magnitude at TSV/liner interface.

Even though the work [27] studied TSV interfacial crack analysis in full-chip scale and provided several design guidelines to suppress mechanical reliability problem in 3D ICs, there are still a lot of open problems to be explored. First of all, all the aforementioned works considered only one silicon substrate die containing TSVs. However, thermo-mechanical stress distribution around TSV can be highly affected by package components [13], hence their impact on the TSV interfacial crack growth behavior needs to be carefully addressed. Also, thermo-mechanical stress level and mechanical reliability problem can be different between stacked dies depending on the distance from C4 bump. Thus, chip/package co-design methodology considering whole stack needs to be studied. In addition, other types of crack induced by TSV such as substrate crack need to be examined to better understand the overall TSV-induced cracking growth behavior.

## VI. Other Manufacturability and Reliability Issues

While the previous sections give some examples of TSV-induced stress, EM, and crack, many of those studies are focused on the TSVs themselves, or on one die out of multi-die stacking. For the entire 3D-IC and packaging, we need to consider all the multi-scale interconnects together. The multi-die stacking, C4 bumps, underfill, and packaging substrate all add mechanical stress to the 3D IC mounted above it in a non-trivial way [28]. Research is needed to build models that show the impact of these packaging elements to the mechanical reliability of the logic and memory dies. In addition, we need to study the interplay between the stress caused by the TSVs in the 3D IC and the one by these packaging elements to analyze the mechanical reliability of the overall chip/package system. This system-level analysis can be used to either update the design

of the 3D IC or package, improve the materials used, or modify the process/assembly steps to tackle the holistic reliability problems. Some interesting manufacturability and reliability issues which can be explored further include:

(1) Stress Modeling: The impact of off-chip package components such as micro bumps, package bumps, and underfill should be considered for the entire thermo-mechanical stress. Most previous works only considered stress induced by CTE mismatch between TSV and substrate. However, these package components, which are much larger than TSV in volume and have different CTE characteristics, could drastically alter stress distribution in on-chip domain. We are examining how they interact with TSVs and affect thermo-mechanical stress in 3D ICs. We are also studying the impact of design parameters such as size of each package element, relative position between these elements, and the number of dies stacked. It will also be interesting to see if the linear superposition principle for the full-chip/package co-analysis of thermo-mechanical stress holds, under what condition.

(2) Crack Analysis: The package components could change stress distribution around TSV significantly, hence crack growth behavior can be altered by these package components. We are investigating how these package elements affect crack growth around TSVs, and identifying key design parameters that influence crack growth most significantly. We are also exploring the feasibility of full-chip/package crack analysis methodology based on DOE and RSM.

(3) Mobility Variations: Not only the difference in materials (and thus CTE) of C4 bumps, underfill, and package substrate, but also the direction and distance between each die and these structures affect the stress map. TSVs and STIs on a die affect stress on the same die mostly in lateral direction; however, these structures affect stress in vertical direction. The closer a die is to the packaging substrate, the more the effect is on the stress it experiences. We are simulating this chip/package structure in 3D ICs and developing additional model for stress and mobility variation caused by these structures.

(4) EM Reliability: The significant size mismatch between these routing resources (C4 bumps, RDL interconnects, local wires/vias) aggravates the EM problem at the smaller scale interconnects due to the steep current density gradient and serious current crowding. This EM problem becomes even worse for 3D IC packages because of the stringent power delivery requirement in 3D ICs. The smaller footprint and higher device density of 3D ICs put higher current demand on each power/ground (P/G) C4 bumps and P/G TSVs that are connected to them. This exacerbates EM issues at this chip/package interface further. We need to investigate these issues and build holistic models and methodologies for full-system-scale analysis/optimization tools for both signal and P/G interconnects.

## VII. Conclusions

In this paper, we have discussed major components of design for manufacturability (DFM) and reliability (DFR) for TSV-based 3D-IC. As the 3D-IC manufacturing processes are still yet to be matured for volume production, early researches of DFM and DFR for 3D-IC will have great value in bridging the gaps between manufacturing process/material, circuit design, and architecture. We expect to see a lot of researches for 3D-IC DFM and DFR, for general-purpose as well as application specific 3D-IC architectures.

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