VLSI CAD for Emerging Nanolithography

David Z. Pan, Jhih-Rong Gao and Bei Yu
Dept. of ECE, The University of Texas at Austin, Austin, TX USA
{dpan, jrgao and bei}@cerc.utexas.edu

***Abstract*— *In this paper, we discuss emerging nanolithography technologies including double/multiple patterning, extreme ultraviolet lithography, electron-beam lithography, and their interactions with VLSI CAD. These technologies all have different manufacturing processes with their own challenges/issues. Meanwhile, nanometer VLSI designs and mask synthesis have to be co-optimized with these process technologies to ensure high product quality (performance/power/area, etc.), yield, and throughput to make future scaling worthwhile. Some recent results will be presented to show the enablement and effectiveness of such design and process integration.**

Index Terms— Multiple Patterning Lithography, Layout Decomposition, Extreme Ultraviolet Lithography, Electric Beam, Layout Optimization

I. Introduction

The semiconductor industry has been stuck with the 193nm lithography even for the most advanced 28nm/22nm nodes now. There are several candidate nanolithography technologies for 14nm, 11nm, 7nm and 1× nm for extreme scaling: multiple patterning lithography (MPL), extreme ultraviolet lithography (EUVL), electron beam lithography (EBL), and so on.

MPL is a natural extension of double patterning lithography (DPL). At the concept level, it just repeats the single patterning lithography by using two or more mask/patterning processes individually to form coarser patterns and then combine them to form finer pitches. Several DPL/MPL technologies have been developed [1]–[4], with different design/process requirements. There are two main types of technologies: litho-etch-litho-etch (LELE) and self-aligned double patterning (SADP). Both of them can be extended for multiple patterning, so we will explain the basic process issues here. LELE splits the original design into two masks when the distance between two patterns is less than minimum colorable distance; otherwise, coloring conflict occurs. As shown in Fig. 1, the different masks are represented by different colors. Coloring conflict can be resolved by inserting stitches to split a pattern into two touching parts. However, stitches lead to yield loss due to overlay error [5]. SADP uses sidewall spacer to help achieve finer pitch and resolution. Fig. 2 shows the general process of SADP. It first generates the core mask. Then unit-width sidewall spacer will be deposited on all sides of the core mask. The second mask (trim mask) will trim out wanted patterns. SADP needs more processing steps [6] than LELE, but has better overlay control. However, SADP does not allow any stitch insertion and neither it allows variable width/spacing in general, thus it puts more layout constraints. All types of DPL/MPL require layout decomposition [8]–[11]. To make design is DPL-compliant, early DPL aware physical design such as DPL-aware routing is necessary [12], [23], [24], [28].

EUVL wavelength is 13.5nm, which is good for lithographic resolution. However, EUVL still has tremendous technical barriers such as lack of power sources and defect-free masks. EUVL has several unique challenges compared with conventional lithography. First, flare is inversely proportional to the square of the wavelength [13], thus EUVL suffers much higher *flare* effect caused by surface roughness and light scattering. Flare will degrade aerial image contrast and wafer pattern uniformity [14] [15]. The second major issue of EUVL is the *3D mask effect* such as mask shadowing and multi-layer reflection because EUVL system is not governed by projection masks (as in conventional optical lithography), but reflective mirroring masks [16] [17]. Other key issues with EUVL include *line edge roughness (LER)* [18] [19] and mask defects.

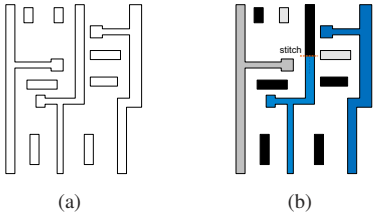

Fig. 1. An example of LELE type MPL. (a) Input layout. (b) Decomposed layouts using three masks.

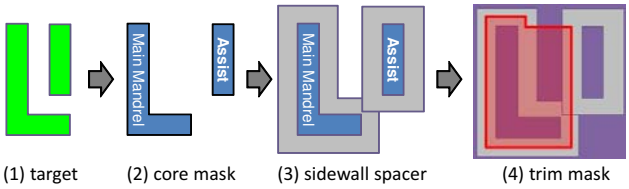

Fig. 2. An example of SADP processing flow for a 2D layout with assist mandrel insertion [7].

EBL is a maskless lithography technology which directly writes layout patterns into the silicon wafer, using charged e-beams. The primary advantage is that the electron wavelength is in the order of 0.001nm which easily beats the diffraction limit of light of other lithography [20]. However, EBL throughput is the biggest bottleneck as the write time is mainly determined by the number of shots.

In the rest of this paper, we will survey recent DPL/MPL works including layout decomposition and routing in Section II. EUVL challenges will be discussed in Section III. CAD for EBL will be discuss in Section IV, followed by conclusion in Section V.

II. CAD for MPL

A. Layout Decomposition

Layout decomposition is a fundamental problem for DPL/MPL which decomposes the original layout into two or multiple masks. Many papers have been published to address the LELE type DPL decomposition problem. Early decomposition algorithms are based on integer linear programming (ILP) to minimize the stitch number and/or conflict number [8] [9]. Yang et al. in [10] proposed a min-cut based, multi-objective layout decomposition framework which can simultaneously consider stitch number minimization, density balancing, and overlay compensation.

Recently several papers have extended the DPL decomposition problem to triple patterning lithography (TPL). At first glance,

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the layout decomposition for TPL seems easier as there are now more masks. However, since the goal of multiple patterning is to achieve finer pitches, there will actually be more features to be packed closer to each other which will form a multi-way conflict. In other words, conflict graphs for TPL will become much denser than those in DPL, and they may be non-planar. In [21], a SAT based decomposition framework was proposed for the contact layer.

In [22], Yu et al. proposed the first general TPL layout decomposition framework which simultaneously minimizes conflict and stitch insertion. They showed that the TPL layout decomposition problem is NP-hard and proposed a semidefinite programming (SDP) based algorithm to achieve good runtime and solution quality. Instead of using a two-bit binary variable to represent three colors, [22] used three unit vectors: $(1,0), (-\frac{1}{2}, \frac{\sqrt{3}}{2})$ and $(-\frac{1}{2}, -\frac{\sqrt{3}}{2})$ to represent three different masks. Note that the angle between any two vectors of the same color is 0, while the angle between any two vectors with different colors is $2\pi/3$. The inner product of two m-dimension vectors $\vec{v_i}$ and $\vec{v_j}$ is defined as $\vec{v_i} \cdot \vec{v_j} = \sum_{k=1}^{m} v_{ik} v_{jk}$. Then for any two vectors $\vec{v_i}, \vec{v_j} \in \{(1,0), (-\frac{1}{2}, \frac{\sqrt{3}}{2}), (-\frac{1}{2}, -\frac{\sqrt{3}}{2})\}$, we have the following property: $\vec{v_i} \cdot \vec{v_j} = 1$ if $i = j$ (possible conflict); $\vec{v_i} \cdot \vec{v_j} = -\frac{1}{2}$ if $i \neq j$ (possible stitch). Based on the vector definition, the layout decomposition problem can be written as a vector programming optimization. Then the discrete vector program is relaxed to the corresponding continuous formulation, which can be resolved as standard semidefinite programming. From the results matrix Y_{ij}, mapping is carried out for mask assignment. Essentially, if Y_{ij} is close to 1, then nodes i and j should be in the same mask; if Y_{ij} is close to -0.5, nodes i and j tend to be in different masks. The results show that with reasonable threshold such as $0.9 < Y_{ij} \leq 1$ for same mask, and $-0.5 \leq Y_{ij} < -0.4$ for different mask, more than 80% of nodes/polygons are decided by the global semidefinite programming optimization. This approximation algorithm is shown to be much more efficient than a conventional integer linear programming (ILP) to simultaneously minimize conflict and stitch.

Even though two features within minimum space are assigned to different masks, unbalanced density would cause lithography hotspots as well as lowered CD uniformity due to irregular pitches [10], all of these may cause yield loss. Different from DPL where two colors can be more implicitly balanced, due to more colors and the bigger solution space, we need to explicitly consider the density balancing in MPL layout decomposition. However, how to address this issue effectively in MPL is still an open problem.

SADP layout decomposition for general 2D patterns is more complicated and less intuitive. The key challenges and differences include: (1) no stitch is allowed in SADP; (2) SADP decomposition may introduce new *assist mandels* not in the original layout to help generate side-wall spacers to achieve intended final patterns; (3) trim mask patterns will also be very different from the original layouts; (4) the overlay error can still happen at the trim mask, though not as severe as LELE.

Ban et al. [7] proposed a systematic flow for SADP layout decomposition for general 2D layouts. The first step for SADP layout decomposition is to pick the core mask. This can be obtained using layout coloring similar to LELE. However, the cost/constraint modeling and objective functions will be very different, e.g., no stitch is allowed in SADP. For general 2D layouts, inserting *assist mandrel* polygons together with the core mask selection is essential because proper assist mandrel insertion can allow certain variable wire widths/spacings and 2D pattern shapes. For example in Fig. 2, an assist mandrel is added on the main mandrel to form the side-wall spacer and secondary pattern (i.e., patterns between spacers formed by main and assist mandrels). Sometimes for 2D layouts, there are inherent conflicts. To address this issue, some ingenuity is needed to merge the original core masks, and later on trim out unwanted patterns. An example is shown in Fig. 3.

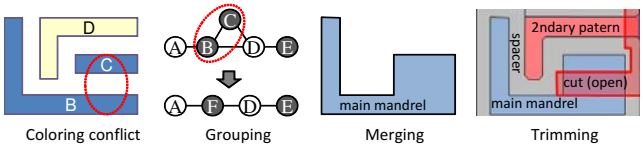


Fig. 3. Grouping and merging coloring for spacer-based multiple patterning

B. MPL Aware Routing

Multiple patterning layout decomposition is a mask synthesis step, which happens after the physical design has been fixed. Though the goal of robust MPL decomposition is to accommodate as much design intent and process constraints as possible, upstream MPL friendly physical design will be important to obtain more flexibility and better quality of results.

There are some studies on LELE type DPL friendly routing [23]–[27]. In [23] detailed routing and layout decomposition are performed simultaneously in a correct-by-construction manner to enhance decomposability. To handle the extra complexity introduced by redundant via, [24] proposed a detailed routing framework to perform DPL and redundant via co-optimization.

For spacer-based multiple patterning lithography, it in general has more restrictive layout requirement. It is still an open research problem how to push the limit of SADP, or even triple patterning (SATP) and quadruple patterning (SAQP), to handle more general 2D layouts with novel physical design and layout decomposition co-optimization. Note that stitch is not allowed in spacer-based MPL to resolve conflict. In [28], a set of SADP-aware layout planning guidelines are presented such as: (1) If both mandrel pattern and trim pattern are conflict-free when being assigned to a route, then the mandrel pattern is preferred; (2) In case that only trim pattern can be assigned for routes with the same routing cost, the one with more spacer protection is preferred; (3) The distance between a trim pattern and a mandrel pattern should not be smaller than a forbidden spacing, although it is legal. To further resolve layout decomposition conflicts, [28] performed proper layer assignment to separate conflicting patterns. By integrating the prescribed routing patterns together with the routing cost, the router can simultaneously perform multi-layer routing and layout decomposition in a correct-by-construction manner.

Different from DPL where the coloring conflicts can be detected by finding an odd-cycle, detecting TPL or the more general MPL coloring conflict *during* routing will be much more complicated due to the higher complexity of conflict graph and higher flexibility for color assignment.

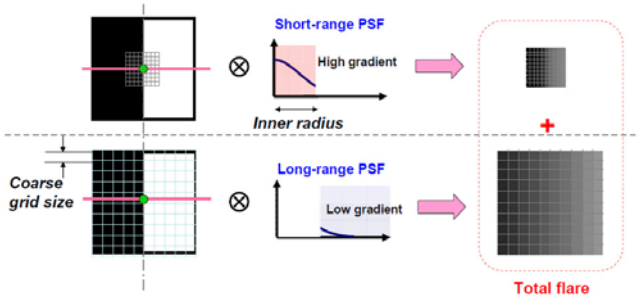


Fig. 4. Total (short and long range) flare kernels in EUV lithography [13]

III. CAD FOR EUVL

It is important to model the variations and defects of EUVL accurately so that the model can be used to guide EUVL proximity correction and EUVL-aware physical design. Several challenging factors for full-chip EUVL modeling, flare, LER, and 3D mask effects, are discussed below.

Flare effect strongly depends on the pattern density. The flare effects can be long-range, medium-range, and short-range flare [29]. To compute the overall flare effect, a *point spread function* (PSF) derived from the surface roughness of the EUV optics can be applied, which can be fitted with a Gaussian function [30], [31]. Then, the aerial image $I(x, y)$ on wafer can be calculated as follows:

$$\begin{aligned} I(x,y) &= I_0(x,y)(1-C) + I_{flare}(x,y) \\ I_{flare}(x,y) &= I_0(x,y) \otimes PSF \end{aligned} \tag{1}$$

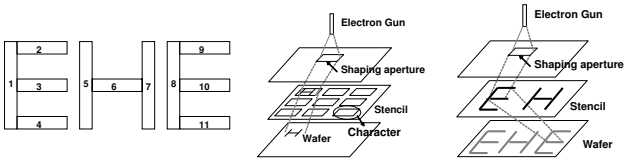
where $I_0(x, y)$ is the areal image without flare, $I_{flare}(x, y)$ is a local flare intensity, and C is a normalization factor to compensate for energy conservation.

A multi-grid structure to model the multi-range flare effects is shown in Fig. 4. Flare contributions from short distances in PSF can be modeled with fine grids because the short range PSF has high gradients, while long range contributions can be calculated with coarser grids. The total flare contribution can be obtained by summing up the multi-range effects [13].

Line end roughness (LER) can be modeled as a power spectral density (PSD) function [32]. While LER is mostly (believed) a random effect, it indeed displays layout-dependent variations as LER depends on aerial image quality. Higher aerial image contrast results in smaller transition region in photo-resist polymer dissolution which reduces LER. In [33], the image log-slope (ILS) is added into LER modeling to consider proximity effects such as pitch spacing for a 32nm process with 193nm lithography. It will be interesting to see how LER for EUV behaves.

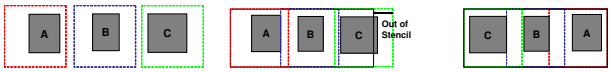
Currently, making a defect-free EUV mask blank is still too costly and impractical, which is one of the main challenges for EUVL. Zhang et. al [34] proposed an efficient layout relocation process to minimize the defect impact on feature boundaries. The idea is to shift the pattern on the blank and move the defects to the spare region where the printing image will not be affected. The pattern relocation problem is formulated into a rectangle overlapping problem and can be optimally solved. The experimental results showed that the patterns affected by the defects can be very much reduced.

More research will be required to model EUVL effects accurately in full-chip scale, such as multi-range flare modeling, 3D mask effect modeling consider layout-dependent variations, and so on. These models can then be further used for EUVL-aware proximity corrections and layout optimizations.



(a) (b) (c)

Fig. 5. EBL with variable shaped beans and character projection.



(a) (b) (c)

Fig. 6. Stencil design and character placement optimization with legal overlapping.

IV. CAD FOR EBL

Conventional variable shaped beam (VSB) system decomposes the entire layout into a set of rectangles, each being shot into resist by some dosage of electron beam. As Fig. 5 (a) shows, the pattern of "EHE" can be divided into eleven rectangles, thus it needs a total of eleven shots. To address this issue, *character projection* (CP) technology [35]–[37] has been invented to improve the throughput. The key idea is to print certain complex shapes in one shot. As shown in Fig. 5 (b) and (c), a library of layout configurations, called *characters* (or *templates*) are prepared on a *stencil* first. During manufacturing, any layout pattern which can be found at the stencil will be chosen and directly projected into the wafer in one shot. For example of Fig. 5 (a), suppose two characters "E" and "H" are pre-designed for the stencil. By adjusting the shaping aperture, we can print the patterns in 3 shots, instead of 11. Due to less beam shots for the same layout, CP system has much higher throughput than VSB. However, the number of characters that can be placed on a stencil is limited due to area and spacing constraints. For those patterns not matching any characters, they are still required to be written by VSB.

It is intuitive that commonly used circuit patterns should be selected as characters for minimizing the total number of shots, hence projection time and throughput. In [38], frequently-used standard cells were greedily chosen as characters, processed by CP technology. Sugihara et al. [39] [40] applied integer linear programming to optimize the throughput, given a set of character candidates. [35]–[37] showed that when individual characters are designed, blanking space has to be reserved in their enclosed rectangular boxes due to e-beam scattering effects, as shown in Fig. 6 (a).

In [41], [42] Yuan and Pan proposed a new problem of e-beam lithography stencil design with *legal* overlapped characters. As shown in Fig. 6, suppose there are three character candidates A-C, and we would like to pack them into a simple stencil. Their blanking spaces are quite different and asymmetric among A, B, and C. If they are placed in the order of A-B-C as shown in Fig. 6 (b), only A and B can fit in the stencil. Pattern C has to be processed by VSB shots. In contrast, if the order is rearranged to be C-B-A as in Fig. 6 (c), all three patterns can fit. This is just a one-dimensional example. For two-dimensional stencil optimization, the complexity will be much higher due to asymmetric patterns. Heuristics including greedy algorithm and simulated annealing were proposed to address both the 1D and

2D stencil planning problems. The experimental results showed that compared to conventional stencil design methodology without overlapped characters, the total projection time is reduced by 51%. In [43] Du et al. provided a character and stencil design framework for inter-cell layout, where certain wire and via patterns are adopted.

V. Conclusion

In this paper, we show several CAD challenges and recent results for emerging nanolithography, including multiple patterning lithography, EUV lithography and electron beam lithography. Since all of these techniques are candidates for 14nm, 11nm, or even 7nm technology node and beyond, we expect to see a lot of research opportunities on addressing both mask and physical synthesis for these emerging nanolithography technologies.

Acknowledgments

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