Chip/Package Co-Analysis of Thermo-Mechanical Stress and Reliability in TSV-based 3D ICs

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ABSTRACT

In this work, we propose a fast and accurate chip/package thermo-mechanical stress and reliability co-analysis tool for TSV-based 3D ICs. We also present a design optimization methodology to alleviate mechanical reliability issues in 3D IC. First, we analyze the stress induced by chip/package interconnect elements, i.e., TSV, μ-bump, and package bump. Second, we explore and validate the principle of lateral and vertical linear superposition of stress tensors (LVLS), considering all chip/package elements. This linear superposition principle is utilized to perform full-chip/package-scale stress simulations and reliability analysis. Finally, we study the mechanical reliability issues in practical 3D chip/package designs including wide-I/O and block-level 3D ICs.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

General Terms

Design

Keywords

3D IC, TSV, stress, mechanical reliability, chip/package co-analysis

1. INTRODUCTION

Most previous works on the thermo-mechanical stress and reliability of TSV-based 3D ICs have been done separately in chip or package domain. The impact of TSV-induced stress due to coefficient of thermal expansion (CTE) mismatch between TSV and substrate materials on device performance [1] and crack growth in TSV [7] were studied in the chip domain. As for the package domain, many works focused on the reliability of package bump (= C4 bump) [9]. Recently, authors in [8] showed the significant impact of package components on the chip domain stress. They proposed a stress exchange file to transfer the boundary conditions from package-level to silicon-level analysis. However, all of these approaches require FEA methods which are computationally expensive or infeasible for full-chip or -package analysis.

To overcome the limitation of FEA method, linear superposition of stress tensors [5] and response surface method [4] were utilized. However, all of these are limited to the chip domain analysis. In this paper, we propose a full-chip/package-scale thermo-mechanical stress and reliability co-analysis flow as well as a design optimization methodology to reduce the mechanical reliability problems in TSV-based 3D ICs. We show the impact of design parameters such as the size and pitch of chip/package interconnect elements and the number of dies in the stack on thermo-mechanical stress and reliability.

The main contributions of this work include the following: (1) Modeling: Compared with existing works, we simulate more detailed 3D IC structures including both chip and package components and study their interaction and impact on thermo-mechanical stress and reliability. (2) Full-chip/package co-analysis: We, for the first time, validate the principle of lateral and vertical linear superposition of stress tensors induced by each chip/package interconnect element such as TSV, μ-bump, and package-bump against FEA simulations. We apply this methodology to generate a stress map and a reliability metric map in full-chip scale. (3) Case study: we study the mechanical stress and reliability issues in practical 3D chip/package designs including wide-I/O and block-level 3D ICs.[1]

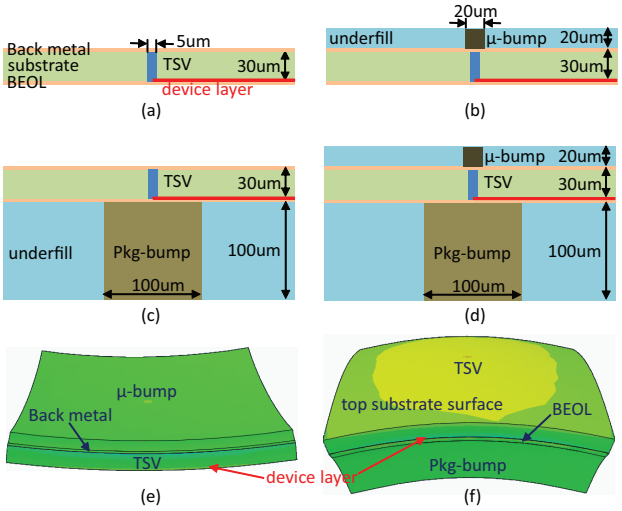

Figure 1: Impact of bumps and underfill on the stress of device layer (= red line). (a) TSV only [5] (b) TSV + μ-bump (c) TSV + package-bump (d) TSV + μ-bump + package-bump. (e) Deformed structure of (b). (f) Deformed structure of (c). Both (e) and (f) are drawn with 10X deformation scale factor.

2. MOTIVATION

We first examine how various chip/package interconnect components interact and alter the thermo-mechanical stress distribution on the *device layer around TSV* caused by the CTE mismatch between

[1]We also explore the impact of TSV/bump placement, size, and pitch on the overall system, and the materials are moved to the Supplemental Section due to the space limit.

DAC '12, Jun 03-07 2012, San Francisco, CA, USA

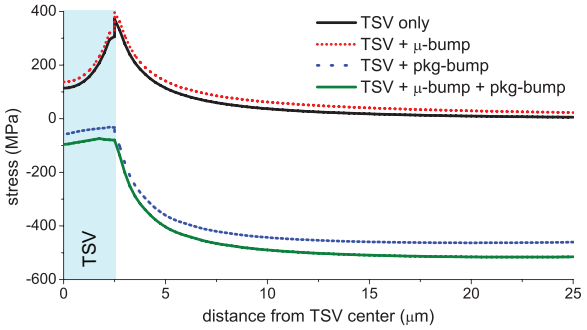

Figure 2: Impact of package components on the stress (σ_{rr}) around TSV on device layer (FEA results).

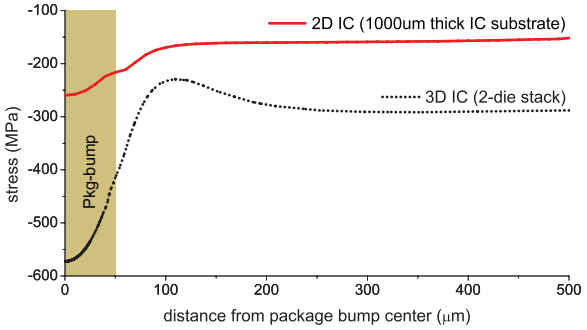

Figure 3: Comparison of impact of package-bump on the device layer stress (σ_{rr}) between 2D IC and 3D IC (2-die stack) (FEA results).

TSV and substrate materials. First, we only consider TSV and substrate which most previous works studied. We employ the same simulation structure used in [5] as shown in Figure 1(a). Then, we add a μ-bump and underfill layer *above* the substrate as shown in Figure 1(b). All structures undergo ΔT = -250°C of thermal load (annealing/reflow 275°C $\rightarrow$ room temperature 25°C). As Figure 2 shows, by adding the μ-bump layer (= dotted red line), we see slightly more tensile (= positive) stress than the TSV-only case (= solid black line). This is because ΔCTE of μ-bump and underfill is 24 ppm/K, while that of TSV and substrate is 14.7 ppm/K, hence the deformation of the entire structure is largely determined by the μ-bump and underfill layer. Since the top side of μ-bump layer is free surface, the entire structure easily bends upward as all the elements shrink from the negative thermal load as shown in Figure 1(e). Thus, the materials on device layer stretch outward, which results in more tensile stress.

On the other hand, if we add a package-bump (= C4 bump) layer *below* the substrate as shown in Figure 1(c), now the entire structure bends downward as shown in Figure 1(f) because package elements are shrinking more than chip elements. The ΔCTE of package bump and underfill is 22 ppm/K. This generates highly compressive (= negative) stress on the device layer. Comparing Figure 1(b) and Figure 1(c), we see that the bending direction depends on which layer shrinks more: in both cases, the bump layers shrink more than the silicon substrate.

Lastly, we include both bump layers as shown in Figure 1(d). In this case, the ΔCTE is almost the same (24 ppm/K on the top, 22 ppm/K on the bottom). However, the overall structure bends down in a similar fashion as shown in Figure 1(f) because of the sheer volume of package bump layer (= shrinking more than the μ-bump layer). This in turn causes compressive stress in the device layer. However, the magnitude is slightly *more* (= solid green line in Figure 2) than the package-bump layer only case (= dotted blue line). One might expect the overall compressive stress would

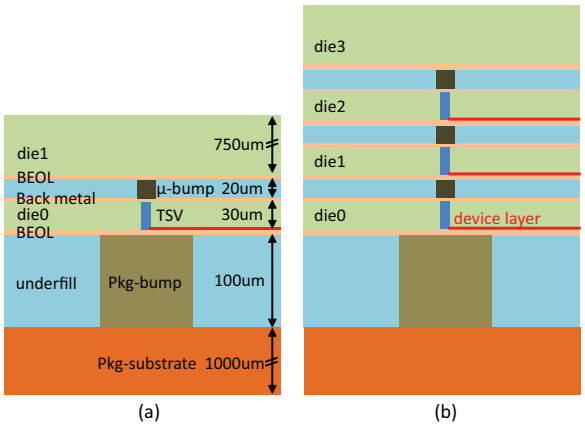

Figure 4: Side view of baseline chip/package simulation structures. (a) 2-die stack (b) 4-die stack.

be less because the μ-bump layer tries to bend upward while the package-bump layer tries to bend downward (= canceling effect). However, this additive effect is because the μ-bump layer eventually bends down and adds more compressive stress to the device layer. Remember that the bending direction of the μ-bump layer is affected by adjacent layers. Since now the deformation of the entire structure is dominated by the package-bump layer, the flexible underfill material in the μ-bump layer easily bends downward. These basic simulations clearly show the importance of considering package element impact on the chip-domain stress distribution.

Figure 3 shows the stress contributions of package bump and underfill layer to the chips (2D vs. 3D) mounted on it. For the 3D IC/package structure, we build a two-die stack chip/package structure similar to Figure 4(a) excluding TSV and μ-bump. This was to examine the impact of package-bump solely. The bottom die (= die0) is thinned, and we examine the device layer of this thin die. One 2D IC/package structure is also created, where we use a single un-thinned die of 1000 μm thickness. We examine the device layer of this un-thinned die. We apply the same thermal load (ΔT = -250°C) for both cases. Figure 3 shows that the 3D IC experiences more severe compressive stress than the 2D IC case. The main reason is the thickness and the flexibility of the die that we are monitoring. Even though the thickness of the entire structure is thicker in 3D IC, the thin die (30 μm thick) and the underfill material above the thin die is much more flexible than the un-thinned substrate in 2D IC. Thus, this thin die is highly affected by the package-bump underneath it. This indicates that the impact of package-bump is more significant in 3D IC.

3. 3D IC/PACKAGE STRESS MODELING

We use the von Mises yield criterion [10] as a mechanical reliability metric for TSVs, which is explained in Section S.1. However, we do not use a specific threshold value for the von Mises criterion in this work, since it is greatly affected by fabrication process.

3.1 3D IC/Package Simulation Structure

Figure 4 shows our simulation structure, where the dimensions of our baseline simulation structures are based on the fabricated and/or published data [2, 8]. In this work, we specifically examine the stress distribution on device layer for each die shown in red lines in Figure 4. Our baseline TSV diameter, height, landing pad size, Cu diffusion barrier thickness, and dielectric liner thickness are 5 μm, 30 μm, 6 μm, 50 nm, and 125 nm, respectively. We use Ti and SiO_2 as Cu diffusion barrier and liner materials. Also, diameter/height of μ-bump and package-bump are 20 μm and 100 μm, respectively, unless otherwise specified. Material properties used for our experiments are as follows: CTE (ppm/K) / Young's modulus (GPa) for Cu = (17/110), Si = (2.3/188), SiO_2 =

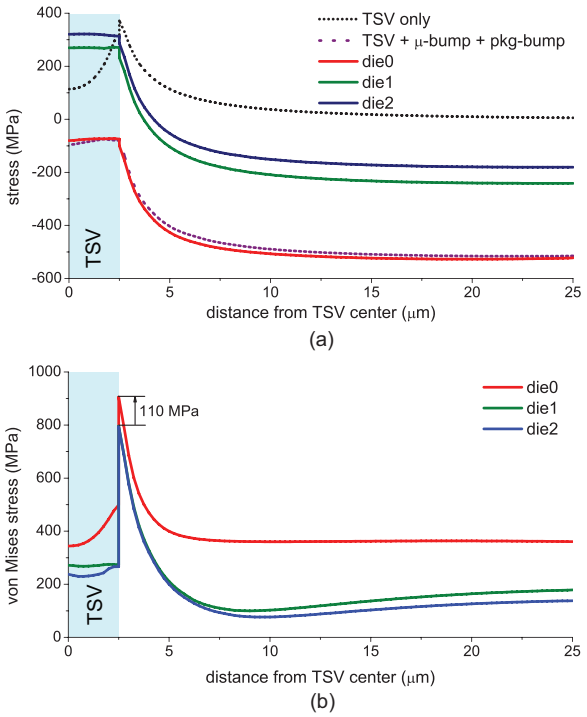

Figure 5: Impact of die stacking on device layer stress (FEA results). (a) σ_{rr} stress on device layer in each die in 4-die stack. (b) von Mises stress in each die in a 4-die stack.

(0.5/71), Ti = (8.6/116), package-bump (SnCu)= (22/44.4), μ-bump ($Sn_{97}Ag_3$) = (20/26.2), underfill = (44/5.6), package substrate (FR-4) = (17.6/19.7).

We use a FEA simulation tool ABAQUS to perform experiments, and all materials are assumed to be linear elastic and isotropic. We also discuss the impact of the anisotropic Si material property on the thermo-mechanical stress and reliability in Section S.4. The entire structure undergoes ΔT = -250°C of thermal load (annealing/reflow 275°C $\rightarrow$ room temperature 25°C) to represent a fabrication process. In addition, all materials are assumed to be stress free at the annealing/reflow temperature.

3.2 Impact of Die Stacking

Previous works on the full-chip thermo-mechanical stress analysis used the same stress pattern for different dies in a multiple-die stack [1, 5]. In this section, for the first time, we examine how the thermo-mechanical stress distribution on the device layer around TSV differs across strata. We employ the four-die stack structure for this purpose. Also, we use only one TSV, μ-bump, and package-bump for each die or layer, respectively, and their center locations are aligned as shown in Figure 4.

First of all, the stress level, the extent of compression or tension, differs significantly across dies as shown in Figure 5(a). The overall stress trend remains similar: the stress is highest at TSV edge and decays then saturates as distance increases from the TSV center. However, the bottom-most die (= die0, solid red line), which is closest to the package-bump layer, shows most compressive stress among three dies containing TSV. This is because the impact of package-bump is most significant in die0 due to their proximity.

Also, as we go to the upper dies, the stress level becomes closer to the case considering only TSV and substrate. We also see that the stress curve of die0 is very close to the case of TSV + μ-bump + package-bump (= dotted purple line), which does not contain the package substrate and un-thinned top die shown in Figure 1(d). This also indicates that the stress level in die0 is mostly determined by package-bump. The stress distribution in die3 (un-thinned top die without TSVs) is almost flat (-110 $\pm$ 5 MPa). Since die3 does not contain any TSVs, there is no local von Mises stress peak (= dangerous region) caused by TSVs. Thus, we only consider the dies containing TSVs in this work.

Moreover, we observe that the mechanical reliability problem is most severe in die0 shown in Figure 5(b). The maximum von Mises stress at TSV edge in die0 is about 110 MPa higher than the upper two dies. This is again mostly due to the package-bump that induces large deformation at the nearest die.

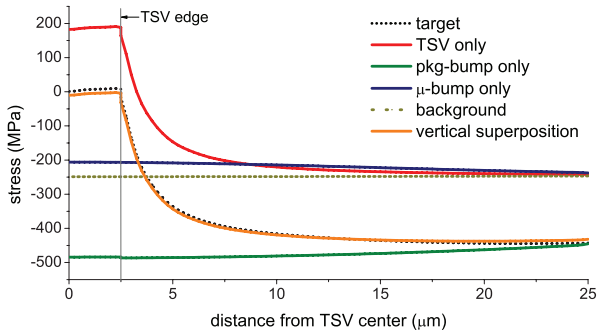

Figure 7: Vertical linear superposition of σ_{rr} stress in a 2-die stack shown in Figure 6

4. HANDLING FULL-CHIP/PACKAGE

FEA simulation for multiple TSVs, μ-bumps, and package-bumps require huge computing resources and time, thus it is not feasible for a full-system-scale analysis. In this section, we present a chip/package thermo-mechanical stress co-analysis flow in full-chip/package scale. We use the principle of lateral and vertical linear superposition of stress tensors from individual TSVs, μ-bumps, and package-bumps to enable a full-system-level analysis. We validate our approach against FEA simulation results. Based on the linear superposition method, we build full-chip stress maps and then compute the von Mises yield metric to assess the mechanical reliability problems in TSV-based 3D ICs.

4.1 Lateral and Vertical Linear Superposition

In [5], authors used the principle of linear superposition of stress tensors to perform a full-chip stress and reliability analysis considering many TSVs. In that case, all stress contributors (= TSVs) are on the same layer, hence we call this lateral linear superposition. However, as we consider the impact of μ-bump and package-bump, which are not in the same layer where TSVs are located, this lateral linear superposition cannot be used alone. Fortunately, the principle of linear superposition is not limited to 2D plane, but applicable to any linearly elastic structures including 3D structures.

Figure 6 illustrates our vertical linear superposition method, which enables us to consider the stress induced by elements which are not in the same layer. We first decompose the target structure into four separate structures: TSV only, package-bump only, μ-bump only, and background which does not contain TSV and bumps. Next, we obtain stress tensors along the red line on device layer affected by each interconnect element separately from FEA simulations. Then, we add up the stress tensors from TSV only, package-bump only, and μ-bump only structures, and subtract twice the magnitude of the background stress tensors since this background stress is already included in previous three structures. If the point under consideration is affected by n components, then we need to substract n-1 times the background stress.

Figure 7 shows the stress distributions from each structure as well as the stress obtained by the vertical linear superposition. We see that μ-bump induces more tensile stress than background and package-bump generates much more compressive stress than background, which is discussed in Section 2. We also observe that even without interconnect elements (= background) device layer is in

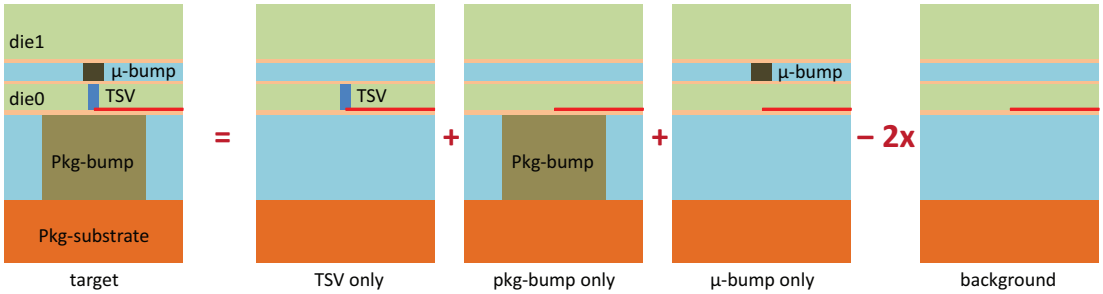

Figure 6: Illustration of vertical linear superposition with a 2-die stack structure. Stress is extracted along the red line on device layer from each structure using FEA tool.

compression due to the shrinking of the underfill material which has the highest CTE (= 44 ppm/K) among all materials in the simulation structure. Most importantly, our vertical linear superposition method matches well with the target stress distribution. Although we see the maximum error (11 MPa) occurs inside TSV, this is inevitable since we ignore the direct vertical interaction between TSV, μ-bump, and package-bump by decomposing the structure. Nonetheless, this error is acceptable for a fast full-system-scale analysis.

To obtain the stress tensor at a point affected by multiple TSVs, μ-bumps, and package-bumps, we apply both lateral and vertical linear superposition (LVLS) as follows:

$$S = \sum_{i=1}^{n_{SV}} S_{TSV\,i} + \sum_{j=1}^{n_{\mu}} S_{\mu B_j} + \sum_{k=1}^{n_{pkg}} S_{pkgB_k} - (n_{TSV} + n_{\mu B} + n_{pkgB} - 1) \times S_{bg} \quad (1)$$

where, S is the total stress at the point under consideration and $S_{TSV\,i}$, $S_{\mu B_j}$, and S_{pkgB_k} are individual stress tensor at this point due to i^{th} TSV, j^{th} μ-bump, and k^{th} package-bump, respectively. S_{bg} indicates the background stress at that point.

4.2 Full-Chip/Package Stress Analysis Flow

We briefly explain how we perform a full-chip/package stress analysis based on the LVLS method. We first build a stress library from FEA simulations. This library contains stress tensors along an arbitrary radial line on the device layer induced by each interconnect element, i.e., TSV, μ-bump, and package-bump, separately. Given locations of TSVs, μ-bumps, and package-bumps, we find a stress influence zone for each element. Beyound this stress influence zone of each interconnect element, the stress induced by the element under consideration is negligible [5]. In our work, we use five times the diameter of each component as a stress influence zone, where stress level is saturated to the background stress level from FEA simulations.

Then, we associate each grid point with all the interconnect elements whose stress influence zone overlaps with the point. Next, we apply the LVLS method at the point under consideration to obtain the stress tensor induced by every component found in the association step. Finally, we compute the von Mises stress to assess the mechanical reliability problem in TSVs. More details of our algorithm is discussed in Section S.6.

4.3 Validation of LVLS

In this section, we validate our LVLS method against FEA simulations by varying the number of TSVs, μ-bumps, and package-bumps as well as their arrangement. We set the minimum pitch of TSV, μ-bump, and package-bump as 10 μm, 20 μm, and 200 μm for all test cases. Stress tensors along the radial line on device layer induced by each interconnect element (stress tensor library) are obtained through FEA simulation with 0.25 μm interval. In our linear superposition method, simulation area is divided into uniform array style grid with 0.1 μm pitch. If the stress tensor at the grid point under consideration is not obtainable directly from the stress library, we compute the stress tensor using linear interpolation with adjacent stress tensors in the library.

Table 1: Von Mises stress comparison between FEA and LVLS for a 4-die stack structure (die0). Error = LVLS - FEA. (At TSV edge, typical von Mises stress level is around 900 MPa.)

# TSV /μ-B /pkg-B	FEA		LVLS		max error (MPa)		
	# node	run time	# grid	run time	inside TSV	TSV edge	outside TSV
1/1/1	754K	1d2h	1M	23s	-11.4	-12.6	7.9
2/2/1	812K	1d2h	1M	26s	-12.7	-13.2	7.3
5/5/2	902K	1d6h	6M	2m43s	-14.1	-15.3	8.2
10/10/4	1.3M	1d20h	9M	6m44s	-23.1	-19.8	9.4
10/10/9	1.4M	2d0h	16.8M	11m11s	-22.5	-20.5	11.9

Table 1 shows some of our comparisons in die0 in a four-die stack, which shows the largest errors among three dies containing TSVs due to its proximity to package-bumps. Also, we only list the cases with the minimum pitches for each component, which again shows maximum errors. First, we observe a huge run time reduction in our LVLS method. Note that we perform FEA simulations using 8 CPUs while only one CPU is used for our linear superposition method. Even though the LVLS method performs stress analysis on a 2D plane (= device layer), whereas FEA simulation is performed on the entire 3D structure, we can perform stress analysis for other planes in a similar way if needed.

The error between FEA simulations and LVLS is very small. Results show that our LVLS method underestimates stress magnitude inside TSV and TSV edge, and overestimates outside TSV, as shown in Figure 7. In general, the most critical region for the mechanical reliability is the interface between different materials, hence TSV edge is most important in our case. Even though the maximum error at TSV edge is as high as -20.5 MPa, its % error is only -2.24 %. Figure 8 shows one test case comparison of von Mises stress between FEA and LVLS. The structure has 10 TSVs (5 μm diameter and 10 μm pitch), 10 μ-bumps (20 μm diameter and 40 μm pitch), and 9 package-bumps (100 μm diameter and 200 μm pitch). It clearly shows our LVLS method matches well with the FEA simulation result.

5. SIMULATION RESULTS

We implement a chip/package thermo-mechanical stress and reliability co-analysis flow based on LVLS in C++/STL. More details can be found in Section S.6. We explore the impact of package-bump and μ-bump on the reliability in full-system scale. Also, we examine the reliability concerns in wide-I/O DRAM and block-level 3D IC designs.

In our experiments, we adopt a regular TSV placement style in which TSVs are placed uniformly across each die or inside TSV blocks with pre-defined pitch. In all cases, the pair of TSV and μ-bump is vertically aligned. Default diameter/height (μm) of TSV, μ-bump, and package-bump are 5/30, 10/10, and 100/100, respec-

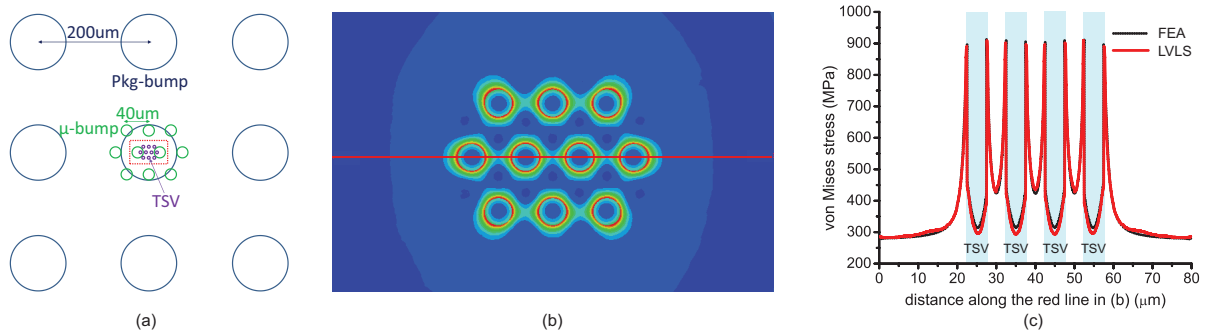

Figure 8: Sample stress comparison between FEA and LVLS. (a) Test structure. (b) Close-up shot of von Mises stress map (using LVLS) taken from the red box in (a) on the device layer in die0 in a 4-die stack. (c) FEA vs. LVLS along the red line in (b).

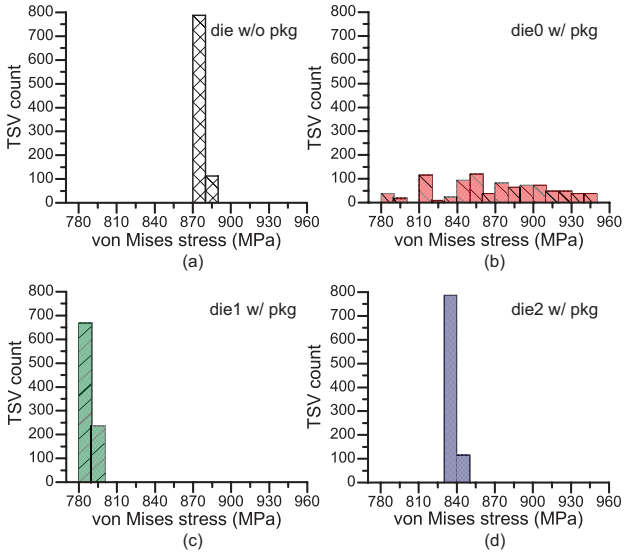

Figure 9: Impact of package components and die stacking on the mechanical reliability of TSVs (900 TSVs in each die).

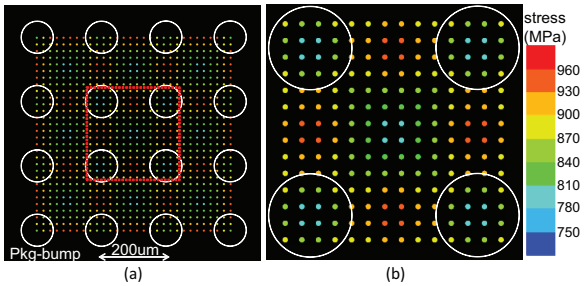

Figure 10: Von Mises stress map for TSVs (die0 in a 4-die stack). Colored dots are TSVs and white circles are package-bumps. (a) Test structure. (b) Close-up shot of red box in (a)

Table 2: Reliability in wide-I/O DRAM.

case	von Mises stress distribution (MPa)					median
	780-810	810-840	840-870	870-900	900-930	(MPa)
(a)	30	114	52	220	608	944.8
(b)	182	842	0	0	0	856.2

tively, unless otherwise specified.

5.1 Impact of Package-Bump and μ-Bump

We first study the impact of package-bump and μ-bump on the mechanical reliability of different dies in a four-die stack. We also compare this to the case without these components as in the previous work [5] as shown in Figure 1(a). In this experiment, the pitch of TSV/μ-bump and package-bump are 20 μm and 100 μm, respectively; the total number of TSV/μ-bump and package-bump are 900 and 16, respectively, as shown in Figure 10(a).

We first observe that unlike the die without package-bumps and μ-bumps (Figure 9(a)) and the upper dies with package components (Figure 9(c) and (d)), TSVs in die0 (Figure 9(b)) experience large variations of von Mises stress across the die. This is because die0 is highly affected by package-bumps underneath it, and hence depending on the relative position between TSVs in die0 and package-bumps the von Mises stresses of TSVs change noticeably.[2]

We also identify that higher von Mises stress occurs around package-bump edge and in between package-bumps due to constructive stress interference shown in Figure 10(b). However, as we see in the center of Figure 10(b), if the distance between TSV and package-bumps is long enough, the von Mises stress of TSV becomes low.

Interestingly, die1 shows lowest von Mises stress level among all cases even though die2 is farthest from package-bumps. This is due to the fact that die2 is affected by the rigid un-thinned top silicon substrate above it. Since die0 is most problematic in terms of the mechanical reliability, we only consider die0 in a four-die stack in the subsequent experiments.

5.2 Case Study I: Wide-I/O DRAM

Wide-I/O based 3D DRAM is fast becoming the first mainstream product that utilizes TSV in 3D ICs, mainly targeting mobile computing applications such as smart phones which need lower power consumption and high data bandwidth. In this section, we evaluate the reliability concerns of TSVs in wide-I/O DRAM. We follow the TSV placement style similar to the work in [6], where TSV arrays are placed in the middle of a chip. We assume that 2x128 TSV array (per memory bank) is placed in the middle of a chip shown in Figure 11. We employ four memory banks and 1024 TSVs in total. We set the pitch of TSV/μ-bump and package-bump as 15 μm and 200 μm, respectively. We compare two cases; (a) Package-bumps are placed right underneath TSV arrays; (b) Package-bumps are placed with 200 μm spacing from TSV arrays. This 200 μm distance is chosen since we see that the effect of package-bump on the TSV reliability is negligible beyond 200 μm in case of the 100 μm diameter package-bump shown in Figure 16.

Table 2 clearly shows that the chip/package co-design can greatly reduce the mechanical reliability concerns in TSV-based 3D ICs.

[2]Note that we see higher von Mises stress level in (Figure 9(a) than the previous work [5] even with the same simulation structure. This is because we use the Young's modulus of 188 GPa for Si instead of 130 GPa in [5] as a worst case scenario. More details are discussed in Section S.4.

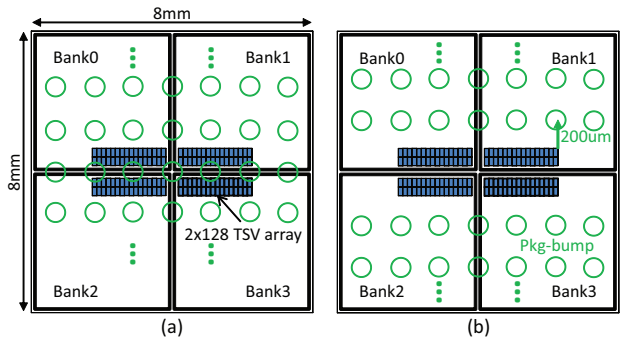

Figure 11: Mechanical reliability in wide I/O DRAM. 1024 TSVs are placed in the middle of a chip. (a) Package-bumps are placed underneath TSV arrays. (b) Package-bumps are placed 200 μm apart from TSV arrays. (not drawn in scale.)

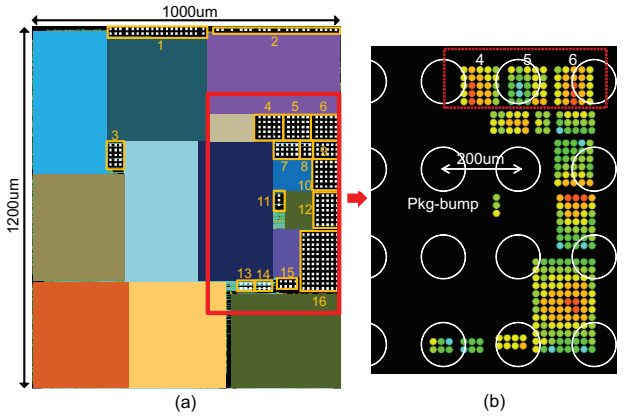

Figure 12: Mechanical reliability in block-level 3D IC. (a) Sample layout of block-level design. (b) Von Mises stress map for TSVs in red box in (a).

With a safe margin of 200 μm (= case(b)), von Mises stress magnitude reduces significantly. Thus, given the TSV placement, we can find safe locations for package-bumps without affecting the package design much, or vice versa.

5.3 Case Study II: Block-Level 3D IC

In this section, we study the reliability issues in block-level 3D designs. 3D block-level designs are generated using an in-house 3D floorplanner which treats a group of TSVs as a block shown in Figure 12. Total 16 TSV blocks (368 TSVs) are used and the TSV pitch is 15 μm. Package-bumps are regularly placed with 200 μm pitch.

Table 3 shows von Mises stress level in selected TSV blocks. We first observe that larger TSV blocks experience more variation of von Mises stress within the TSV block. This is because the distance between each TSV in the block and package-bumps can vary more than small TSV blocks, which is a key factor that affects the reliability of TSVs. We also see that TSV blocks with the same size can show quite different characteristics depending on the distance to the nearest package-bump. For example, although TSV block 4, 5, and 6 are all 5x5 TSV blocks and are located side-by-side, TSV block 5 shows the lowest von Mises stress level. However, its standard deviation of von Mises stress is highest among three blocks. We observe lower von Mises stress if TSV is placed near the package-bump center or far away from it; however, we see higher stress in TSV located around package-bump edge shown in Figure 16 in Section S.5. In case of TSV block 5, most TSVs are near the package-bump center, which lowers von Mises stress level.

Table 3: Mechanical reliability in block-level 3D IC. TSV blocks are shown in Figure 12.

TSV block #	# TSV	von Mises stress (MPa)				blk-bump dist (μm)
		max	min	avg	std dev	
3	5x3	901.0	811.1	859.5	26.0	96.4
4	5x5	939.6	853.5	902.6	24.0	67.6
5	5x5	908.6	816.0	858.7	33.3	24.1
6	5x5	942.3	874.4	910.4	22.0	91.4
11	3x1	896.6	855.9	871.0	18.2	39.3
16	12x8	943.7	806.0	877.2	33.6	90.7

However, at the same time a few TSVs are around the package-bump edge, which increases the standard deviation of von Mises stress inside the TSV block.

From this experiment, we observe two possible ways to reduce the mechanical reliability problems in block-level 3D designs: (1) Assign TSV blocks right above package-bump center locations if possible. (2) Place package-bumps outside the TSV block locations with a safe margin such as outside the red box in Figure 12(a). However, other design constraints such as package area and the required number of pins sholud be carefully considered as well.

6. CONCLUSIONS

In this work, we showed how package elements affect the stress field and the mechanical reliability on top of the TSV-induced stress in 3D ICs. We observed that the mechanical reliability of TSVs in the bottom-most die in the stack are highly affected by packaging elements, and that effect decreases as we go to the upper dies. We also presented an accurate and fast full-chip/package stress and mechanical reliability co-analysis flow based on the principle of lateral and vertical linear superposition of stress tensors (LVLS), considering all chip/package elements.

7. ACKNOWLEDGMENTS

This work is supported in part by the National Science Foundation under Grants No. CCF-1018216, CCF-1018750, the SRC Interconnect Focus Center (IFC), SRC Task 2239.001 and 2238.001 (CADTS), and SRC task 2244.001 and 2243.001 (SEMATECH 3D EC).

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S. SUPPLEMENTAL MATERIAL

In this section, we provide basic concepts and thorough modeling results of thermo-mechanical stress and reliability analysis. We first introduce the concept of stress tensor and von Mises yield criterion. Then, we discuss the impact of the thickness of both package substrate and un-thinned top substrate on the stress. We also model how the alignment of TSV, package-bump, and μ-bump affect the mechanical reliability, and observe that relative distance between TSV and package-bump is the key factor that determines the reliability of TSV. In addition, we examine how the anisotropic Si material property affects the stress and reliability compared with the isotropic Si, and why we use the isotropic Si material property as a worst case scenario in our work.

We also present details of our full-chip/package stress and reliability analysis flow. Then, we provide extensive full-chip/package analysis results which show the impact of TSV/bump size and pitch on the reliability. In general, smaller size and larger pitch of each interconnect element help reduce the mechanical reliability problem of TSV-based 3D ICs. However, other design constraints such as the area of chip and package should be carefully considered.

S.1 Stress Tensor & Von Mises Criterion

To help understand stress modeling results, we introduce the concept of a stress tensor. Stress at a point in a body can be described by the nine-component stress tensor:

$$\sigma = \sigma_{ij} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix}$$

where, the first index i indicates that the stress acts on a plane normal to the i axis, and the second index j denotes the direction in which the stress acts. If index i and j are same we call this a normal stress, otherwise a shear stress. Since we adopt a cylindrical coordinate system in this modeling for the cylindrical TSV, μ-bump, and package-bump, index 1, 2, and 3 represent r, θ, and z, respectively.

In order to evaluate if computed stresses indicate possible reliability concerns, a critical value for a potential mechanical failure must be chosen. The von Mises yield criterion is known to be one of the most widely used mechanical reliability metric [10]. If the von Mises stress exceeds a yielding strength, material yielding starts. Prior to the yielding strength, the material will deform elastically and will return to its original shape when the applied stress is removed. However, if the von Mises stress exceeds the yield point, some fraction of the deformation will be permanent and non-reversible even if applied stress is removed [5].

There is a large variation of yield strength of Cu in the literature, from 225 MPa to 3.09 GPa, and it has been reported to depend upon thickness, grain size, and temperature [10]. In this work, rather than selecting a specific value of yield stress for Cu TSV, we show how von Mises stress level changes under various circumstances. The yield strength of silicon is 7000 MPa, which will not be reliability concerns for the von Mises yield criterion.

The von Mises stress is a scalar value at a point that can be computed using components of a stress tensor shown in Equation (2).

S.2 Impact of Thickness of Substrate

In this section, we study the impact of the thickness of package substrate and un-thinned top silicon substrate on the thermo-mechanical stress. We use a 1 mm thick package substrate and a 750 μm thick un-thinned top die as a baseline structure.

We first vary the package substrate thickness from 0.75 mm to 3 mm, and monitor the stress around TSV on device layer in die0 in a four-die stack structure. We observe that stress becomes more compressive as thickness increases, but the difference is almost indistinctive shown in Figure 13(a). This is mainly because this package substrate is already much thicker than other layers, hence its increased thickness impact on device layer is negligible.

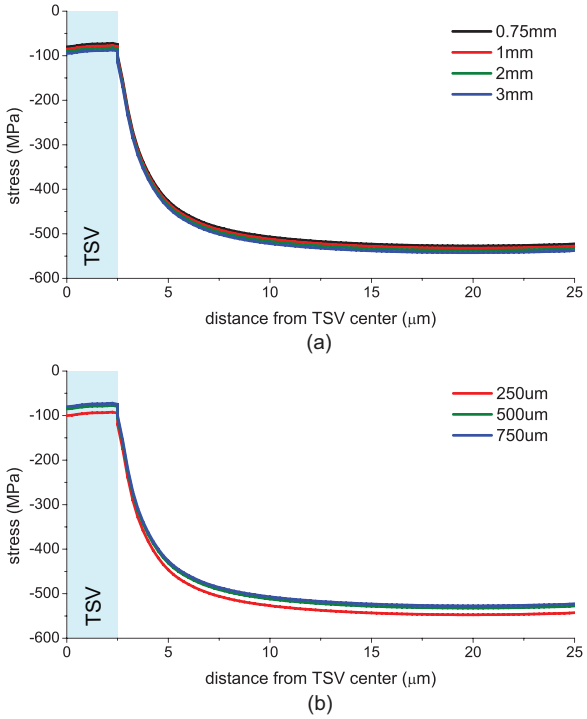

Figure 13: Impact of package substrate and un-thinned top die thickness on stress (FEA results). (a) Impact of package substrate thickness. (b) Impact of un-thinned top die thickness.

We also change the thickness of the un-thinned top die from 250 μm to 750 μm, and observe that thinner die induces more compressive stress. This is because thinner die is more flexible as we see in the thin die case, and hence helps the entire structure bend more easily. However, still the differene is not significant. Thus, we use the baseline 1 mm thick package substrate and 750 μm thick un-thinned top die in our experiments.

S.3 Impact of Multiple Die Stacking

We now examine the stress magnitude in each die with a different number of die stacking. Figure 14 shows stress distributions in die0 with a two-die, a three-die, and a four-die stack. As more dies are stacked, more compressive stress occurs in die0 due to the additional stress from dies above. However, we see that this difference becomes smaller as we go to the upper dies, e.g., die1 stress in a three-die and a four-die stack.

S.4 Isotropic vs. Anisotropic Si Property

Up to this point, all materials are assumed to be isotropic for simplicity. However, Si is an anisotropic material with elastic behavior that depends on which crystal direction the structure is being stretched. The possible values of Young's modulus (E), which is a measure of stiffness of a material, for Si range from 130 to 188 GPa, and those for Poisson's ratio (ν) range from 0.048 to 0.4. Thus, the choice of this value can affect analysis results significantly [3]. In this section, we examine the impact of anisotropic material property of Si on the stress distribution compared with the isotropic Si material property.

$$\sigma_v = \sqrt{\frac{(\sigma_{xx}-\sigma_{yy})^2 + (\sigma_{yy}-\sigma_{zz})^2 + (\sigma_{zz}-\sigma_{xx})^2 + 6(\sigma_{xy}^2+\sigma_{yz}^2+\sigma_{zx}^2)}{2}} \quad (2)$$

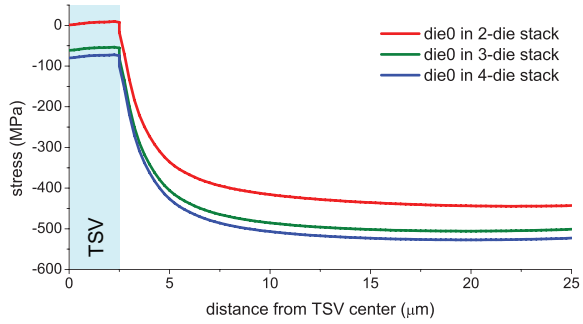

Figure 14: σ_{rr} stress on die0 with a different number of die stacking.

Elasticity is the relationship between stress (σ) and strain (ϵ). Hooke's law describes this relationship in terms of stiffness C, i.e., $\sigma = C\epsilon$. For isotropic uniaxial cases, stiffness C can be represented by a single value of Young's modulus E, and the equation takes the form of $\sigma = C\epsilon$. In an anisotropic material, a fourth rank stiffness tensor with 3^4 = 81 terms is required to describe the elasticity. Fortunately, due to the cubic symmetry of Si, the elastic properties can be expressed in terms of orthotropic material constants. An orthotropic material is one which contains at least two orthogonal planes of symmetry, and Si, with cubic symmetry, can be described this way. The orthotropic elasticity of Si can be expressed with reference axes of a standard (100) Si wafer, which are [110], [$\bar{1}$10], and [001],

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} = \begin{bmatrix} c1 & c5 & c6 & 0 & 0 & 0 \\ c5 & c1 & c6 & 0 & 0 & 0 \\ c6 & c6 & c2 & 0 & 0 & 0 \\ 0 & 0 & 0 & c3 & 0 & 0 \\ 0 & 0 & 0 & 0 & c3 & 0 \\ 0 & 0 & 0 & 0 & 0 & c4 \end{bmatrix} \begin{bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{yz} \\ \epsilon_{zx} \\ \epsilon_{xy} \end{bmatrix}$$

where, orientation specific constants c1, c2, c3, c4, c5, c6 are 194.5, 165.7, 79.6, 50.9, 35.7, and 64.1, all in GPa, respectively. This stiffness tensor translates to E_x = E_y = 169 GPa, E_z = 130 GPa, ν_{yz} = 0.36, ν_{zx} = 0.28, and ν_{xy} = 0.064 [3].

Figure 15 shows the stress comparison between anisotropic and isotropic Si (Young's modulus = 188 GPa for all directions) material properties. We see that the normal stress component becomes less compressive and the von Mises stress is lower with the anisotropic Si compared with the isotropic Si case. This is largely due to the fact that we use the maximum Young's modulus for the isotropic Si case. With higher Young's modulus Si substrate becomes stiffer, hence higher stress builds up at the TSV/substrate interface. In this work, even though anisotropic Si property is more realistic, we use the isotropic Si property as a worst case scenario.

S.5 Impact of TSV and Bump Alignment

In this section, we explore the impact of alignment between TSV, μ-bump, and package-bump on the mechanical reliability of TSVs. We first examine the impact of relative position between TSV/μ-bump and package-bump. We use a two-die stack structure in which center locations of TSV, μ-bump, and package-bump are aligned as shown in Figure 16(a). Then we shift both TSV and

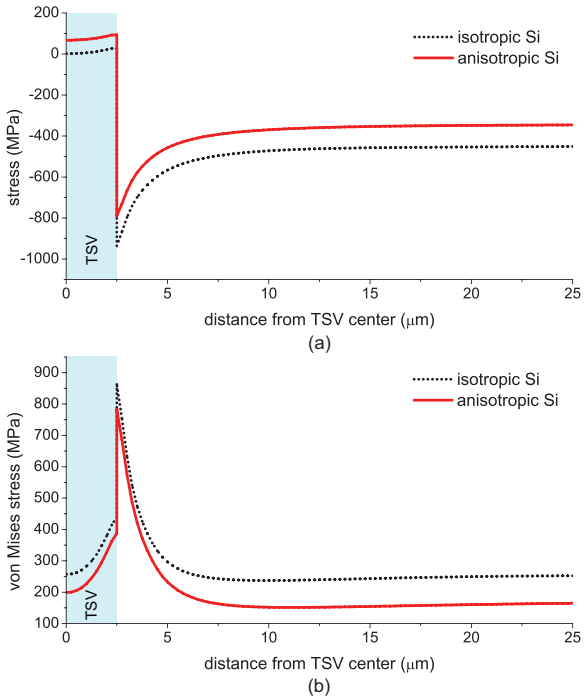

Figure 15: Impact of silicon material property on stress (FEA results). (a) $\sigma_{\theta\theta}$ stress. (b) Von Mises stress.

μ-bump together from the package-bump center with a 25 μm step and monitor the von Mises stress at the right edge of TSV.

Figure 16(c) shows that the von Mises stress is maximum around package-bump edge region and then decreases and saturates as distance increases. The difference between minimum and maximum is as high as 11.1 %. As Figure 3 shows, the highest stress gradient occurs around package-bump edge which results in the highest deformation of the structure near this region. Hence, this higher deformation causes more severe mechanical reliability problem in TSV.

We also see the decrease in von Mises stress near the package-bump center. This is because the material around this area is the same (= package-bump material), hence its deformation is relatively smaller than the edge which is the interface between two different materials.

We also examine whether relative position between μ-bump and TSV/package-bump affects the mechanical reliability of TSV. We fix the location of TSV and package-bump whose centers are aligned, then move μ-bump only with a 5 μm step up to 30 μm and monitor the von Mises stress at TSV edges. We observe the similar trend as before. However, the difference between minimum and maximum is only 6.5 MPa (0.8 %), which is negligible. Thus, we identify that the relative position between TSV and package-bump is a critical factor that affects the mechanical reliability of TSV.

S.6 Full-Chip/Package Analysis Algorithm

In this section, we discuss details of our full-system-scale thermo-mechanical stress and reliability analysis flow. First, based on the

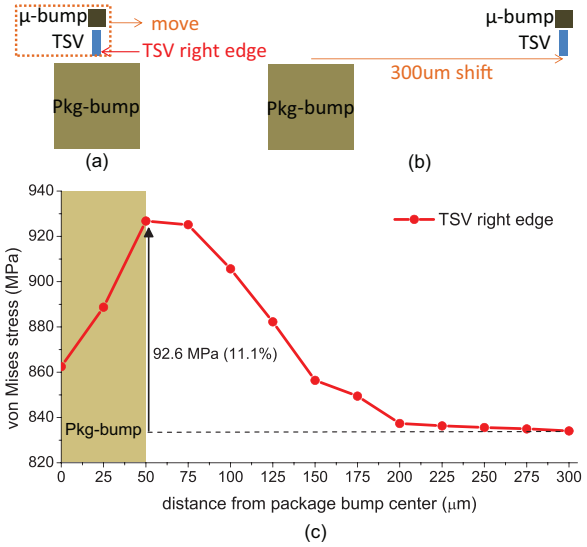

Figure 16: Impact of relative position between TSV/μ-bump and package-bump on von Mises stress. (a) Initial position. (b) Final position where TSV/μ-bump are shifted by 300 μm from package bump center. (c) Von Mises stress at TSV edge along the distance between TSV/μ-bump and package-bump (FEA results).

observation that the stress field induced by a single TSV, a μ-bump, and a package-bump in isolation is radially symmetrical due to their cylindrical shape, we obtain stress tensors for each interconnect component along an arbitrary radial line on device layer from their center location in a cylindrical coordinate system. To evaluate the stress tensor at a point affected by multiple interconnect elements, a conversion of a stress tensor to a Cartesian coordinate system is required. This is due to the fact that we extract stress tensors from these interconnect components whose center position is the origin in the cylindrical coordinate system; hence we cannot perform a vector sum of stress tensors from each component which has a different center location.

Then, we compute the stress tensor at the point of interest by adding up the stress tensors from TSVs, μ-bumps, and package-bumps that affect this point. We set a stress influence zone of TSV, μ-bump, and package-bump 25 μm, 100 μm, 500 μm from the center of each component, which is five times the diameter of each component, respectively. This is because the magnitude of each stress tensor component saturates well before this distance, hence there is a negligible impact from the interconnect element beyond this stress influence zone.

Let the stress tensor in Cartesian and cylindrical coordinate system be S_{xyz} and $S_{r\theta z}$, respectively.

$$S_{xyz} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix}, S_{r\theta z} = \begin{bmatrix} \sigma_{rr} & \sigma_{r\theta} & \sigma_{rz} \\ \sigma_{\theta r} & \sigma_{\theta\theta} & \sigma_{\theta z} \\ \sigma_{zr} & \sigma_{z\theta} & \sigma_{zz} \end{bmatrix}$$

The transform matrix Q is the form:

$$Q = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

where, θ is the angle between the x-axis and a line from the center of each interconnect element to the simulation grid point. A stress tensor in a cylindrical coordinate system can be converted to a Cartesian coordinate system using conversion matrices: $S_{xyz} = QS_{r\theta z}Q^T$ [5].

input : TSV list T, pkg-bump list P, μ-bump list M, stress library
output: stress map, von Mises stress map
for *each TSV t, pkg-bump p, and μ-bump m in T, P, and M* **do**
  $(it, ip, im) \longleftarrow$ FindStressInfluenceZone(t, p, m)
  for *each point it′, ip′, and im′ in it, ip, and im* **do**
    $it'.TSV \longleftarrow it$
    $ip'.pkg\text{-}bump \longleftarrow ip$
    $im'.\mu\text{-}bump \longleftarrow im$
  end
end
for *each simulation point r* **do**
  if $r.TSV \neq \emptyset$ || $r.pkg\text{-}bump \neq \emptyset$ || $r.\mu\text{-}bump \neq \emptyset$ **then**
    for *each* $(t, p, m) \in (r.TSV, r.pkg\text{-}bump, r.\mu\text{-}bump)$ **do**
      $(dt, dp, dm) \longleftarrow distance(t, p, m, r)$
      $S_{cyl}(t, p, m) \longleftarrow$ GetStressTensor(dt, dp, dm)
      $S_{cyl}(t, p, m) \longleftarrow S_{cyl}(t, p, m) - BGstress$
      $\theta(t, p, m) \longleftarrow$ GetAngle$(line\ tr, pr, mr, x\text{-}axis)$
      $Q_(t, p, m) \longleftarrow$ SetConversionMatrix$(\theta_t, \theta_p, \theta_m)$
      $S_{Cart}(t, p, m) \longleftarrow$
      $Q_(t, p, m) S_{cyl}(t, p, m) Q_(t, p, m)^T$
      $r.S_{Cart} \longleftarrow r.S_{Cart} + S_{Cart}(t, p, m)$
    end
  end
  $r.S_{Cart} \longleftarrow r.S_{Cart} + BGstress$
  $vonMises(r) \longleftarrow$ ComputeVonMises$(r.S_{cart})$
end

Algorithm 1: Full-Chip/Package Stress and Reliability Analysis Flow (LVLS)

Our full-system-scale thermo-mechanical stress and reliability analysis flow is shown in Algorithm 1. We first start to find a stress influence zone from each TSV, μ-bump, and package-bump. Then, we associate the points in the influence zone with the affecting interconnect elements. Next, for each grid point under consideration, we look up the stress tensors from each interconnect component found in the association step, and subtract background stress from the stress tensor. Then, we use the coordinate conversion matrices to obtain stress tensors in the Cartesian coordinate system. We visit an individual TSV, μ-bump, and package-bump affecting this simulation point and add up their stress contributions. After visiting all the components effecting this point, we add one background stress back. Once we finish the stress computation at the point, we obtain the von Mises stress value using Equation (2).

S.7 Impact of Bump Size

In this section, we study the impact of package-bump and μ-bump size on the reliability. First, we vary the package-bump diameter/height from 100 μm to 300 μm, while fixing the package-bump pitch and the TSV/μ-bump count and pitch as 400 μm, 1600, and 20 μm, respectively. Table 4 shows that the number of TSVs experiencing higher von Mises stress increases with larger package-bumps due to the larger deformation of a stack and the increased package-bump circumference where highest von Mises stress occurs. However, in the 300 μm package-bump case, there are more TSVs with lower von Mises stress (780 - 870 MPa) than the 200 μm package-bump case. As discussed in Section S.5, TSVs lo-

Table 4: Maximum von Mises stress distribution of TSVs with different size of package-bump and μ-bump. (die0 in four-die stack with 1600 TSVs)

von Mises stress (MPa)	pkg-bump size (μm)			μ-bump size (μm)		
	100	200	300	10	20	30
780-810	31.2%	17%	17.8%	4.2%	5.6%	0%
810-840	33.8%	18%	27.8%	6.9%	6.3%	6.9%
840-870	19%	14%	17.2%	22.9%	22.2%	15.3%
870-900	14%	28.5%	12.2%	21.5%	22.9%	18.1%
900-930	2%	20.5%	13.5%	27.1%	22.9%	22.9%
930-960	0%	2%	10%	17.4%	20.1%	36.8%
960-	0%	0%	1.5%	0%	0%	0%
median (MPa)	824.6	871.7	848.2	893.3	890.1	908.0

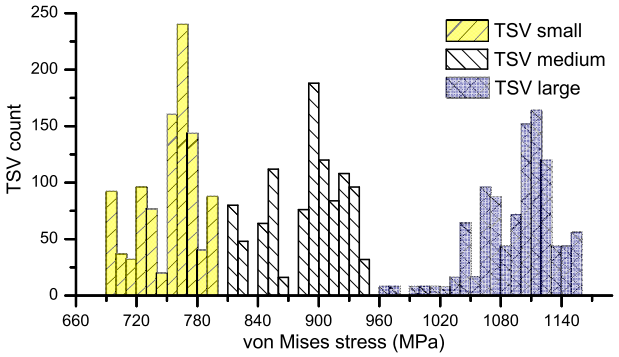

Figure 17: Impact of TSV size on von Mises stress distribution of TSVs. (die0 in four-die stack with 1024 TSVs)

cated near the package-bump center region show lower von Mises stress than those around package-bump edge. Hence, with larger package-bumps more TSVs reside near the package-bump center, which results in lower von Mises stress level for these TSVs.

We now vary the μ-bump size, and use a 100 μm package-bump with a 200 μm pitch. Note that since we align center locations of TSV and μ-bump, we set the TSV pitch as 35 μm to accommodate the largest μ-bump diameter of 30 μm. We observe that larger μ-bump causes more TSVs to experience higher von Mises stress. However, this μ-bump size impact is less significant than the package-bump size.

S.8 Impact of TSV Size

In general, package-bumps and μ-bumps generate global stress distribution, while TSVs create local stress distribution. Therefore, TSV size and pitch are still critical factors that affect the mechanical reliability problem in TSVs even with the presence of other interconnect elements. In this section, we investigate the effect of TSV size. We use three different sizes of TSV with the same aspect ratio of 6; TSV small ($H/D = 15/2.5$ μm), TSV medium ($H/D = 30/5$ μm), and TSV large ($H/D = 60/10$ μm), where H/D is TSV height/diameter. We set the pitch of TSV and package-bump as 25 μm and 200 μm, respectively for all cases.

Figure 17 shows that smaller TSVs reduce the von Mises stress level significantly. This is mainly because larger TSV induces higher stress level at TSV edge due to the sheer volume of TSV. Also, the magnitude of normal stress components decay proportional to $(D/2r)^2$, where r is the distance from the TSV center. In other words, larger TSV affects larger area, hence increases stress level around it more than smaller TSV.

Table 5: Impact of package-bump and TSV/μ-bump pitch on von Mises stress. (die0 in four-die stack with 900 TSVs)

von Mises stress (MPa)	pkg-bump pitch (μm)			TSV/μ-bump pitch (μm)		
	200	250	300	15	25	35
780-810	4.7%	6.3%	19.5%	0.6%	4.6%	7.1%
810-840	4.7%	21.5%	27.0%	3.1%	4.6%	6.9%
840-870	21.9%	27%	31.6%	19.1%	21.6%	22.9%
870-900	19.5%	33.2%	20.3%	23.5%	20.9%	21.5%
900-930	24.2%	12.1%	1.6%	26.4%	23.7%	17.5%
930-960	25.0%	0%	0%	23.4%	24.6%	24.1%
960-	0%	0%	0%	3.9%	0%	0%
median (MPa)	897.9	863.9	844.1	901.8	897.9	893.2

Table 6: Details of the mechanical reliability in TSV blocks in Figure 12.

TSV block #	# TSV	von Mises stress (MPa)				blk-bump dist (μm)
		max	min	avg	std dev	
1	2x19	909.0	798.5	839.6	34.0	96.4
2	1x20	921.9	805.2	846.5	35.2	97.9
3	5x3	901.0	811.1	859.5	26.0	96.4
4	5x5	939.6	853.5	902.6	24.0	67.6
5	5x5	908.6	816.0	858.7	33.3	24.1
6	5x5	942.3	874.4	910.4	22.0	91.4
7	3x5	915.2	855.3	891.3	16.6	61.0
8	3x2	887.2	854.3	865.4	11.2	78.4
9	3x5	889.3	802.5	856.3	24.6	106.0
10	6x5	933.6	812.7	857.8	36.0	111.2
11	3x1	896.6	855.9	871.0	18.2	39.3
12	7x5	952.7	797.1	871.3	43.9	98.8
13	2x3	879.4	807.4	836.9	24.4	100.7
14	2x3	834.7	800.7	820.4	10.9	114.8
15	2x4	909.6	888.5	895.3	7.1	73.9
16	12x8	943.7	806.0	877.2	33.6	90.7

S.9 Impact of Pitch

In this section, we explore the effect of package-bump and TSV/μ-bump pitch on the reliability. We employ a 100 μm package-bump and change its pitch from 200 μm to 300 μm. The pitch of TSV/μ-bump is set to 25 μm. Table 5 shows that larger package-bump pitch reduces the von Mises stress level noticeably by reducing constructive stress interference between package-bumps. However, we cannot arbitrarily increase the package-bump pitch considering the package size increase given the required number of pins.

We also examine the impact of TSV pitch on the von Mises stress. In this case, we set the package-bump pitch as 200 μm. In Table 5, we see that larger TSV pitch reduces von Mises stress level. However, there is not much difference between 25 μm and 35 μm pitch cases. This is because the stress influence zone of a 5 μm diameter TSV is 25 μm, hence there is a negligible difference between these two cases in terms of the stress induced by TSVs solely. Thus, in this case, the von Mises stresses of TSVs are largely determined by relative position between TSVs and package-bumps. Therefore, the proper TSV placement considering the locations of package-bumps is a key design knob to mitigate the reliability concerns in TSV-based 3D ICs.

S.10 Full Details of Table 3

Table 6 shows the details of the missing TSV blocks in Table 3.