Electromigration Study for Multi-scale Power/Ground Vias in TSV-based 3D ICs

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***Abstract*—Electromigration (EM) in power distribution network (PDN) is a major reliability issue in 3D ICs. While the EM issues of local vias and through-silicon-vias (TSV) have been studied separately, the interplay of TSVs and conventional local vias in 3D ICs has not been well investigated. This co-design is necessary when the die-to-die vertical power delivery is done using both TSVs and local interconnects. In this work, we model EM for PDN of 3D ICs with a focus on multi-scale via structure, i.e., TSVs and local vias used together for vertical power delivery. We study the impact of structure, material, and pre-existing void conditions on EM-related lifetime of our multi-scale via structures. Experimental results demonstrate that our EM modeling can effectively capture the EM reliability of the entire multi-scale via in 3D PDN, which can be hard to achieve by the traditional EM analysis based on the individual local via or TSV.**

I. Introduction

Electromigration (EM) is one of the major reliability concerns in advanced IC technology [1]. It refers to the transfer of metal atoms due to the electron current, and is becoming more challenging as feature size shrinks. For EM, local vias in between metal layers of IC have been regarded as EM-prone structures, and have been actively studied [1]–[3]. Meanwhile, EM for through-silicon-vias (TSVs) in 3D IC technology has drawn lots of attention as well, both for modeling [4]–[8] and measurement [6], [9], [10].

In a 3D power distribution network (PDN), local vias often bridge power and ground TSVs, particularly with via-first/middle approach. Jung et al. [11] showed that an array of stacked local vias can exist on top of the TSV landing pad for a 3D PDN as appears in Figure 1. Because this *multi-scale via* (MSV) including a TSV and array of local vias is essential to 3D PDN system, EM issues of MSV needs to be fully studied for reliable 3D ICs. Nonetheless, there has been little effort to study EM issue of the MSV structure in 3D PDN. Frank et al. [9] showed measured data of EM failure in via-first/middle TSV samples, but they used extended M_1 wires to connect the local vias with the landing pad, which can cause a higher IR-drop for PDN, rather than directly placing the local vias on top of the TSV landing pad. Choi et al. [10] showed that EM can occur at the MSV structure, but did not analyze EM failure time as a combined effect of EM of local via and TSV. To the best of our knowledge, there has been no work to model EM of MSV considering both EM in local vias and that in TSV.

In this paper, we study EM robustness of 3D PDN with the MSV structure that includes via-first/middle TSV and stacked local vias. Overall, our contributions are summarized as follows:

- We propose an efficient EM modeling flow for multi-scale vias (MSVs) in 3D PDN.
- We investigate the impact of material property, number and size of local vias, initial void condition on EM-induced failure time of MSV structure.
- We study the interplay between EM of local vias and EM of TSV, and analyze the overall impact on EM of the MSV structure.

The rest of the paper is organized as follows. After introducing the background of this study in Section II, we show our EM modeling methods for MSV in Section III. We then investigate the impact of various factors on failure time of MSV structure in Section IV.

II. Preliminaries

A. 3D PDN Structure

Figure 1 presents power distribution network (PDN) of 3D ICs with via-first/middle TSVs [11]. We define *multi-scale via*, or *MSV*, as a structure composed of multiple local vias and a TSV. In an MSV, local vias are connected to a TSV landing pad in one of the BEOL layers, as shown in Figure 3. On M_1 landing pad of a via-first/middle TSV, an array of local vias (V_1) is directly connected. MSV structures frequently appear in 3D PDN because local vias directly bridging power mesh and TSVs can achieve minimal IR-drop, especially with via-first and via-middle TSVs. With via-last TSVs, on the contrary, MSVs are unnecessary because TSV landing pads abut power mesh on the top metal. In this work, we limit our scope to 3D PDN with MSV structures.

B. Basics of Electromigration

Electromigration (EM) is a wear-out failure mechanism for metal interconnects [3]. EM failures are often caused by the interconnect voiding from metal atomic diffusion. This diffusion is driven by the strong flow of electrons, and the strength of electron flow, denoted as current density, is intensified as feature size shrinks, thereby aggravating the EM problem [3]. The vacancy flux due to EM can be expressed with multiple driving forces such as current density, stress gradient and vacancy concentration, as shown by Eqn. (1) [12].

$$\vec{J}_v = -D_v \left(\nabla C_v - C_v \frac{eZ^*}{kT} \rho \vec{j} + C_v \frac{f\Omega}{kT} \nabla \sigma \right), \qquad (1)$$

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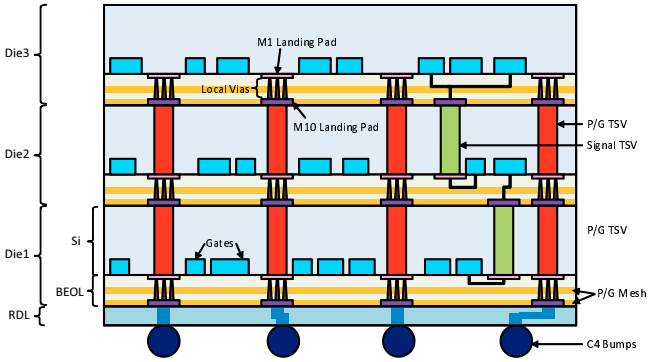


Fig. 1. Power distribution network of 3D ICs with via-first/middle TSVs [11]. Three dies are stacked with face-down, and power/ground TSVs are vertically connected with stacked local via arrays [11].

Here, J_v is vacancy flux, D_v is effective vacancy diffusivity, C_v is vacancy concentration, ρ is electrical resistivity of the material, $\vec{j}$ is current density, e is electron charge, f is vacancy relaxation ratio, Ω is atomic volume, σ is hydrostatic stress, k and T are Boltzmann constant and absolute temperature, respectively. The effective vacancy diffusivity D_v is expressed by Arrhenius equation [12], which shows exponential relationship with temperature,

$$D_v = D_o \cdot exp(\frac{-Ea}{kT}) \tag{2}$$

where Ea is activation energy and D_o is initial diffusivity.

On the right side of Eqn. (1), the second term is the most dominant one that is affected by the current density $\vec{j}$, while other two factors are of secondary importance. Usually the first term can be assumed to be negligible [4]. Moreover, if current density and wire length jL is larger than critical Blech product $(jL)_c$ (which is usually true in PDN mesh), we can neglect the third stress effect term [13]. Thus, vacancy flux can be simplified as

$$\vec{J_v} = D_v C_v \frac{eZ^*}{kT} \rho \vec{j}. \tag{3}$$

Eqn. (3) and (2) will be used for our EM model to simulate void growth in Section III.

Within dual-damascene copper interconnects, line-via interface is the most EM-critical spot [3]. Depending on the current direction, there are two distinctive categories of EM failure [2]; 1) downstream EM (i.e. *line depletion*) and 2) upstream EM (i.e. *via depletion*). With downstream EM, electrons flow from via top to bottom (current flows from bottom to top), and voids are generated beneath the barrier, at the interface of via trench and the lower metal line [1], [2]. Example of voids from downstream EM is shown in Figure 3. On the other hand, with upstream EM, electrons and migrated atoms flow from the bottom to the top of a via, and voids appear inside via trench [1], [2].

Previous studies showed that via-line interface indeed is a site where EM-induced voids appear frequently [9], [14], as shown in Figure 2. With downstream EM, both local vias and TSV can have voids under via structure, right under the barrier structure. Figure 3 illustrates downstream EM of the

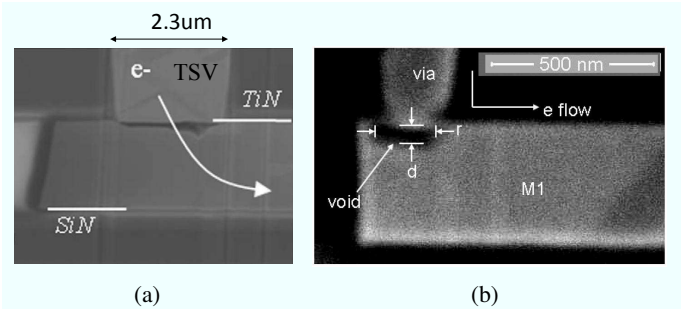


Fig. 2. Void from downstream EM by Focus Ion beam-Scanning Electron Microscopy (FIB-SEM); (a) a void under the TSV [9], (b) a void under local via (V_1) [14].

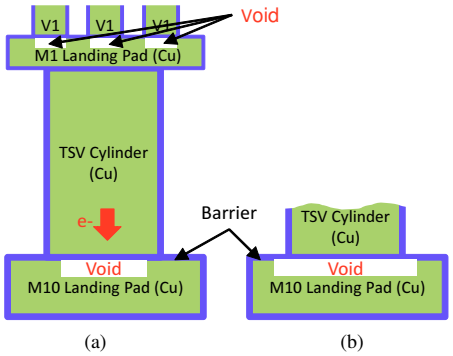


Fig. 3. MSV structure and voids from downstream EM. EM-induced voids are located under the bottom barrier of each TSV and local via. (a) a TSV void smaller than TSV cylinder, (b) a larger TSV void.

MSV structure, with voids under the local vias as well as TSV. Although our algorithm can be utilized to analyze both upstream and downstream EM, in this work, we focus on downstream EM for MSV structure.

For the failure criterion, we use 10% resistance increase from initial resistance value of MSV structure. Previous EM work used either percentage resistance increase (e.g. 10%) [4], [6] or fixed amount resistance increase (e.g. 10Ω) as their failure criteria [15]. We use percentage resistance increase because it gives a more comparable failure times for vias with different initial resistance. Although 10% increase of resistance of structure may not lead to shut-down of entire power/ground network, it means that EM problem has already been initiated and EM-induced problem of the PDN, such as IR-drop increase, can be expected at this point. Estimation of IR-drop can be also used as the failure criterion, but it should be done in the full-chip level simulation, which is beyond the scope in this work.

EM can be generally explained as a two-phase process, void nucleation followed by void growth. However for deep sub-micron copper interconnects, it is reasonable to assume very short void nucleation time because it is nearly impossible to have void-free adhesion between copper and barrier/liner material [1]. The entire failure time can be largely dominated by void growth than void nucleation.

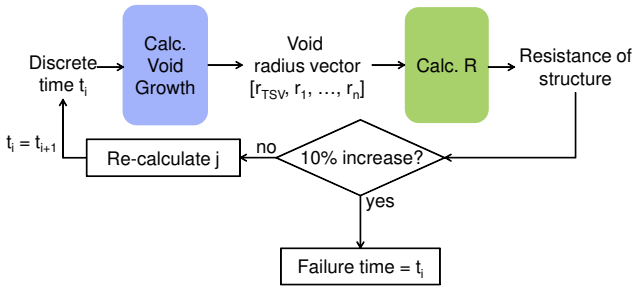


Fig. 4. Flowchart of proposed EM modeling algorithm.

III. Modeling of Electromigration for Multi-scale Vias in 3D PDN

This section discusses our modeling algorithm for EM-related lifetime of multi-scale vias (MSVs) in 3D PDN. We present our EM modeling algorithm summarized in Figure 4. This algorithm uses discrete time with small time step, and calculates the degree of void growth under a via using function named *Calculate Void Growth* (Section III-A). Once we get the vector of void radius for each TSV and local vias, we calculate the resistance of entire MSV structure using function *Calculate Resistance* (Section III-B). Since the failure criterion is 10% increase of resistance from the initial resistance, as we explained in Section II, we check the resulting resistance to see whether it exceeds our failure criterion at each time step. Once it is over the failure criterion, our algorithm reports current time step as the *failure time*. Otherwise, we re-calculate current density of each via, and repeat the cycle.

A. Calculating void growth

Get Void Growth function accepts its input as current time step, void size and current density of each via from previous time. The output of this function, void radius vector, contains radius of a cylindrical void under the barrier of the MSV structure as shown in Figure 3. For example, if a MSV contains four V_1 local vias, void radius vector becomes $[r_{TSV}, r_1, r_2, r_3, r_4]$, where r_{TSV} and r_i represent void radius of TSV and i^{th} V_1, respectively.

For void growth beneath the TSV barrier, previous work [4], [6] used cylindrical void model. Because slit-like voids under the via tend to grow in radial direction, we can assume that cylindrical voids have fixed thickness and grow toward radial direction only, which is similar to other works [4], [6].

For void location, we assumed the worst case, the case when the initial void is located at the center of a via, similarly to previous work [4], [6]. This case is the worst in terms of EM reliability because the void blocks the entire via area in the shortest time.

According to work in [4], [6], void growth can be expressed by the rate of vacancies captured by a void. Void volume formed by infinitesimal time dt can be expressed as the following:

$$dV = \alpha f \Omega A J_v dt \tag{4}$$

where α is the ratio of vacancies captured by the void, A is area under flux effect, and J_v is the vacancy flux [4]. In Eqn. (3), de Orio et al. [4] assumed constant area, A, no matter how big the void radius is. However, the area under vacancy flux that contributes to void growth should change as void size grows. Because we assume cylindrical void grows just in radial direction, only the area around the circumference of a void should be responsible for absorbing vacancies, since that is the *front line of void growth*. Figure 5 shows our concept of cylindrical void growth. Unlike previous work [4], we put *vacancy absorbing area* A in Eqn. (4) as follows,

$$A = 2\pi r_{void} \epsilon. \tag{5}$$

Thus, vacancy absorbing area A becomes a function of void radius r_{void}. dV at Eqn. (4) should be equal to the infinitesimal void volume represented with dotted line in Figure 5, then it can be expressed as

$$dV = \alpha f \Omega A J_v dt = 2\pi \delta r_{void} dr, \tag{6}$$

and thus

$$dr = \frac{\alpha f \Omega A J_v dt}{2\pi \delta r_{void}}, \tag{7}$$

where J_v and A are given by Eqn. (3) and Eqn. (5), respectively. All the parameters we use are presented in Table I. Unlike other work [4], [6], we re-calculate current density of each via for each time step to get feedback from the grown voids.

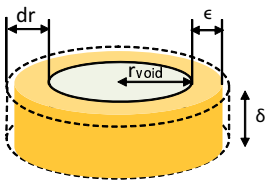


Fig. 5. Cylindrical void under the via. r_{void} is current void radius, dr is infinitesimal void radius growing during time dt, ϵ is effective radius that governs effective cross area A for absorbing vacancies.

TABLE I
Parameter values for EM modeling of MSVs.

Parameter	Description	Value
r_{TSV}	TSV Cu radius	$1.15um$ [6]
l_{TSV}	TSV height	$15.0um$ [6]
$tb_{TSV,side}$	TSV TaN thickness, side	$25.0nm$ [6]
$tb_{TSV,bot}$	TSV TaN thickness, bottom	$45.0nm$ [6]
δ_{TSV}	TSV void thickness	$5.0nm$
LP_{TSV}	TSV landing pad size	$3.6um \times 3.6um$
$t_{LP,M1}$	TSV M_1 landing pad thickness	$0.13um$ [16]
$t_{LP,M10}$	TSV M_{10} landing pad thickness	$2.0um$ [16]
$r_{V1,total}$	V_1 total radius	$32.5nm$ [16]
l_{V1}	V_1 height	$120.0nm$ [16]
$tb_{V1,bot}$	V_1 TaN thickness	$5.0nm$
$r_{V1,Cu}$	V_1 Cu radius	$27.5nm$
δ_{V1}	V_1 void thickness	$1.0nm$
T	Temperature	$453K = 180\ ^\circ C$
ρ_{Cu}	Cu resistivity	$2.73 \times 10^{-8} \Omega m$ at $180\ ^\circ C$
ρ_{TaN}	Barrier (TaN) resistivity	$3.0 \times 10^{-6} \Omega m$ at $180\ ^\circ C$
k	Boltzmann const.	1.38×10^{-23}
α	Ratio of captured vacancies	1.0 [4]
f	Ratio of vacancy volume	0.4 [12]
Ω	Atomic volume	1.182×10^{-29} [12]
D_o	Initial diffusivity	0.0047
Ea	Activation Energy	$0.9eV = 1.44 \times 10^{-19} V$ [6]
Z^*	Effective charge const.	1.0 [4]
e	Electron charge	$1.6 \times 10^{-19} C$
j_o	Initial current density of TSV	$2.5 \times 10^{10} A/m^2$ [6]

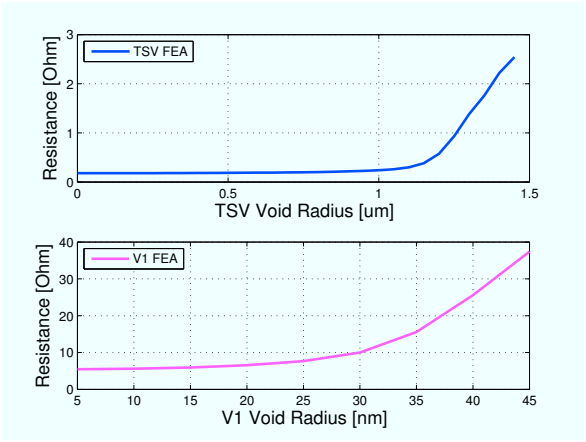


Fig. 6. Relationship between void radius and resistance, for the TSV (top) and for the V_1 (bottom) from FEA simulation. We use TSV radius as 1.15um, and V_1 radius as 27.5nm, thus a void larger than via radius increases the resistance dramatically.

B. Calculating resistance of multi-scale via

Next step of our EM modeling algorithm is to calculate resistance of the MSV, given the void sizes from the previous step. Here we suggest *LUT–based resistance network* model for the MSV. Our approach contains two steps. First we build look-up tables (LUTs) with finite element analysis (FEA) tool to derive resistance of TSV and local via with voids, and then we use resistance network to calculate the total resistance of MSV. We use two different sets of LUTs for TSV and local via, and then utilize them for resistance network. The advantages of our LUT-based resistance network approach are: 1) easy extension to various condition such as different number of vias, because we use accurate FEA results and superpose them for entire resistance 2) fast and accurate results, because LUTs can enable fast reference and interpolation from simulation results. Use of LUTs provides several orders of magnitude faster access to simulation results than doing simulation with FEA for every input void size. Accuracy loss with LUT is limited because the range of input void size is mostly confined to the size of a via and resistance can be assumed to be continuous function of the void size. To derive resistance of a MSV with certain void size, we use industrial FEA tool, COMSOL Multiphysics. Figure 6 shows an example of void radius and resistance of a TSV and a local via (V_1) from the FEA simulation. All the other parameters are from Table I.

To derive resistance of the whole structure, we construct simple resistance network as illustrated in Figure 7. Since local vias are on the same TSV landing pad, they can be represented as parallel resistance network.

With resistance values of vias retrieved from LUTs, we can now calculate the resistance of the entire MSV structure. For resistance values derived by referring to LUTs (R_i for a local via, and R_{TSV} for TSV), total resistance of the MSV (R_{MSV}) with a single TSV and n local vias is as follows:

$$R_{MSV} = \frac{\prod_{i=1}^{n} R_i}{\sum_{i=1}^{n} R_i} + R_{TSV} \ , i \in [1, n] \tag{8}$$

Note that this method can calculate the resistance of the entire structure well regardless of void size distribution among vias.

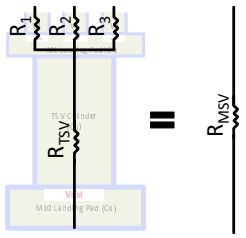


Fig. 7. Resistance network of the TSV and the local via array. Since local vias are connected to the same TSV landing pad, they can be represented as parallel resistance network.

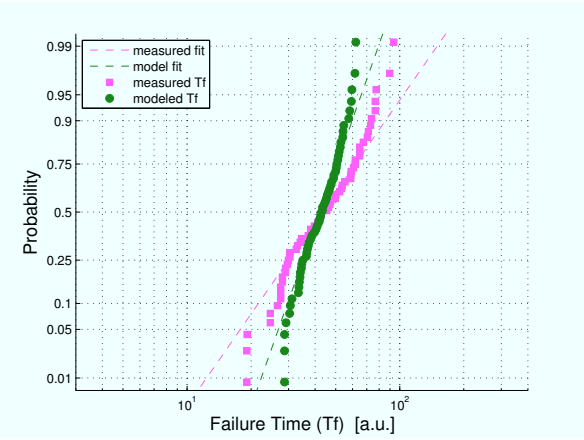


Fig. 8. Comparison of modeled EM-induced failure time against measured data [6] on a log-normal probability plot.

For instance, our algorithm can even be applied to an extreme case where some vias do not have any void at all while others have large voids.

C. Evaluation of our model

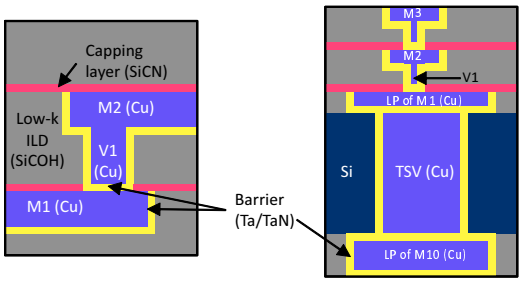
We evaluate our modeling method by benchmarking its results against previous measurements of EM-induced failure time for TSV [6] and local via [15]. To the best of our knowledge, no such measurement study has been done for the entire MSV structure that we can compare our result to. However, we can expect that our modeling approach can provide a reasonable estimate of failure time for the entire structure if modeled failure time of individual components (i.e. TSV and the local via) corresponds with the measured time.

For the comparison of TSV modeling, we apply the parameters used for modeling are the same as the experimental condition in [6]: temperature as $300°C$, current density as $2.5\text{MA}/cm^2$, TSV shape as square of $2.3um \times 2.3um$. Since the work in [6] extracts *effective barrier resistivity* values from their measurement samples, we use their extracted barrier resistivity values to give variation of failure time, similarly to a previous modeling work [4]. Other parameters are as shown in Table I. Figure 8 shows EM-induced failure time distributions from measured data and from our modeling. Although our modeling deviates from measurement result at both extremes, the modeled results around the median corresponds well with the measured data.

Similarly to TSV, we compare our modeled failure time of local vias to the measured data [15]. We use the same physical

TABLE II
COMPARISON OF MODELED FAILURE TIME AND THE MEDIAN OF MEASURED DATA [15], WHEN $j = 2.50\text{MA}/cm^2$.

	Ours	Measured [15]
t_{50} [hrs]	89.0	90.5



(a) (b)

Fig. 9. Schematics of via structures: (a) local via between M_1 and M_2 [17], (b) MSV including via-first/middle TSV [9] and local vias stacked on top of landing pads. Barrier layer (yellow in this figure) is located at the bottom of both local vias and the TSV.

structure as the measurement: we use an additional local via and a M_1 wire, set temperature as $295°C$, set failure criterion as 10Ω increase from the initial resistance. We model failure time with the same current density they use, $2.50\text{MA}/cm^2$. Other parameters for EM model are remained same as in Table I. Table II shows comparison of our modeling result against median failure time t_{50} of measurement [15]. The failure time values closely follows the modeled data.

Together with TSV comparison result, this result suggests that our model is effective in estimating EM-induced failure time with various types of vias, thus it could provide reasonable estimation with MSV structure. For the rest of this paper, we will use this model to evaluate EM induced failure time, with parameters shown in Table I, unless specified otherwise.

IV. STUDY ON EM OF MULTI-SCALE VIAS WITH VARIOUS FACTORS

This section explores several factors that affect EM-induced failure time. One factor of our interest is the material property, more specifically barrier resistivity. We also discuss other structural factors, such as the number of local vias on a TSV, and the size of a local via that is subject to the via design rule of the technology node. Lastly, we study how initial void size of a TSV can affect the failure time of entire MSV structure. Throughout the section, we assume 45nm technology [16].

Our EM modeling algorithm has been implemented with Python programming language, and all the experiments are performed on a machine with 2.93GHz Intel quad-core Xeon X5670 CPU, 71GB of memory, Red Hat Enterprise Linux 5.9. Its running time is dependent on the time step size and the detected failure time. In our experiments, we set the step size so that the number of time steps until the failure time is in between a thousand and ten thousand. This provides comparable results across simulation runs and running time of maximum 30 seconds for each simulation.

A. Study on barrier resistivity

Figure 9 shows schematic view of vias in dual-damascene copper process [9], [17]. For both of TSVs and local vias, tantalum (Ta) or tantalum nitride (TaN) can be used as barrier material at the sidewall and the bottom of via structure. This barrier prevents diffusion of copper to inter-layer dielectric, and enhance adhesion of copper. Although various materials may be used as the barrier material, such as Ta/TaN, TaC, TiN, TiC, WC [1], we limit the scope of our study to TaN due to its wide use. Because the barrier acts as the physical obstacle to atomic flux (zero atomic flux at the boundary [1]), migrated copper atoms from the via trench cannot cross the barrier, which facilitates void growth under the barrier with downstream EM.

TABLE III
RESISTIVITY OF TaN ACCORDING TO PARTIAL PRESSURE OF NITRIDE DURING MANUFACTURING [18].

N_2 pressure	0.0%	5.0%	10.0%	20.0%	30.0%
ρ_{TaN} [1e-8Ωm]	95	254	702	2810	14800

TABLE IV
THE EFFECT OF BARRIER RESISTIVITY ρ_{TaN} ON FAILURE TIME Tf OF MSV.

ρ_{TaN}[1e-8Ωm]	Tf [hrs]
200	1300
300	1214
500	1136
1000	1042
2000	992
3000	967
5000	939
10000	917

Resistivity of barrier material is difficult to express with a constant. In Table III, we show resistivity variation of barrier material TaN which is usually generated by partial pressure of nitride during manufacturing [18]. We note barrier resistance can vary greatly depending on the partial pressure of nitride. In fact, it is hard to express barrier resistivity value of certain barrier structure with a single number because of the variation in the material proportion of compounds as well as in the microstructure such as the grain size and the orientation [1]. Instead of looking at certain values, we observe the impact of wide range of barrier resistivity values on EM failure time of MSV structures.

Based on our model discussed in Section III, we observe the effect of TaN barrier resistivity on EM failure time of MSVs. For the experiments, we set initial void radius as $0.1um$ for a TSV, $1nm$ for local vias, and assume 676 local vias on top of the TSV landing pad[1]. Other parameters are specified in Table I.

The result, presented in Table IV, shows decreasing failure time, i.e. more vulnerability to EM, as resistivity of barrier increases. With the existence of a void under barrier, the current has to detour through the barrier. This detour creates concentration of current in smaller area of the barrier, which magnifies the effect of barrier resistivity, and it contributes to overall resistance increase from void growth. Since our failure criterion involves the relative amount of resistance change, increased resistivity reduces the time to failure.

[1]676 is the maximum number of V_1 local vias that can be packed within 3.6um×3.6um TSV landing pad, assuming 45nm technology for V_1.

TABLE V
THE EFFECTIVE OF BARRIER RESISTIVITY ρ_{TaN} ON FAILURE TIME Tf OF MSVS WITH VARYING RATIO OF VOID-FREE LOCAL VIAS.

ρ_{TaN}[1e-8Ωm]	Tf by V_1 voids only [hrs]	Tf by both TSV void and V_1 voids [hrs] (%: V_1s w/o void)						Tf by TSV void only [hrs]
		0%	10%	20%	50%	80%	90%	
200	1311	1300	1594	4806	6658	7189	7269	7328
300	1222	1214	1411	2856	5839	6456	6561	6650
500	1150	1136	1264	1544	4825	5644	5792	5914
1000	1053	1042	1136	1294	3550	4711	4919	5089
2000	1006	992	1058	1167	2533	4075	4286	4444
3000	989	967	1038	1125	2247	3792	4075	4250
5000	967	939	1017	1092	2025	3561	3842	4075
10000	942	917	997	1072	1850	3406	3683	3911
avg. ratio of Tf	1	0.98	1.10	1.73	3.42	4.49	4.68	4.82

B. Impact of Void-free local vias

Because dual-damascene copper interconnect is known to have zero or small nucleation time, we have assumed that all the local vias and the TSV have nucleated voids that can be grown. However, it is meaningful to see how failure time of MSV changes according to the number of local vias without a void because sets of local vias may exhibit diverse void growth tendency, and a more advanced technology may be able to suppress void nucleation.

Our study with void-free local vias is shown in Table V. Each value represents failure time with a given barrier resistivity and void-free ratio. The result shown in the previous section (Table IV) corresponds to the column with 0% void-free ratio. The second column represents an extreme case when all the local vias have growing voids while TSV has no such void, and the last column shows another extreme when only the TSV has growing voids and all the local vias do not have voids at all. Columns in between show failure time of MSV when both local vias and TSV have growing voids due to EM, with varying ratio of void-free local vias.

If all the local vias and the TSV have their own void due to the EM, we get the worst failure time as shown in the column with 0%. In this case, the overall failure time is driven by the local via voids rather than the TSV void. However, with more void-free local vias, influence of TSV void gets stronger. Since failure time of the TSV void-only case (last column) is much longer than failure time of the local via voids-only case (second column), if more and more vias do not have any void at all, the entire MSV would become much robust and can achieve EM reliability close to a TSV.

Our findings evince the advantage of our approach. Depending on the void condition of vias, failure time of MSV can range from the failure time of the case with local via voids only to that of the TSV void only. Because these diverse void conditions cannot be addressed by other EM models, such as models that only concern local vias or those only for TSVs, our proposed EM modeling for MSV structures is essential to understand the interplay between multiple voids across local vias and the TSV.

C. Study on number of local vias

The size of a TSV is gigantic (a few um) in comparison to a local via (a few tens of nm). If we use just single local via to connect to TSV landing pad for power delivery, extremely high current crowds to the tiny local via and can have immediate failure from EM even at the room temperature. For current load balancing, it is proper to assume multiple local vias on the TSV landing pad for a MSV. In this section, we examine the impact of the number of local vias connected to a TSV. We use 676 vias as the maximum number of local vias in a MSV, observing the design rules [16]. Other than the number of local vias, all the other parameters are still the same as Table I. Here we assume Gaussian distribution for current density between testing MSVs[2].

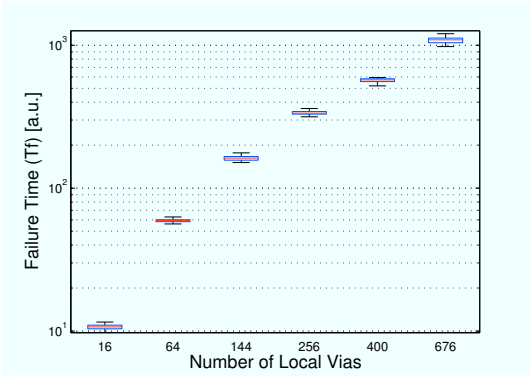


Fig. 10. Impact of the number of local vias on failure time. For each case, 30 samples are used with current density variation. Boxes denote 25 and 75 percentile, while bars are min/max values.

More local vias on a TSV mean more load balancing of current, which eventually extend the failure time of a MSV. This tendency is shown in Figure 10, which is estimated by our EM model (Section III). Increased reliability with more local vias indicates that we can achieve more robust 3D PDN system if we have more local vias connected to the TSV landing pads. We note that the failure time is improved by orders of magnitude when we increase the number of local vias from 16 to 676.

D. Trade-off between via size and number

We have investigated the impact of the number of vias on failure time in Section IV-C, assuming local vias have the minimum size in V_1 layer. The underlying premise is that a TSV landing pad is located on M_1 layer if we have via-first/middle approach for TSV manufacturing. However, via-middle TSV technology makes it possible to build TSV during BEOL process, which places landing pad somewhere between M_1 and M_{10}. With the process, vias connected to a TSV landing pad may become much larger, which may reduce the number of vias, as shown in Figure 11. In this section, we

[2] $j = j_o \times \frac{N(100,\sigma^2)}{100}$ where $\sigma = 4$. Here j stands for current density.

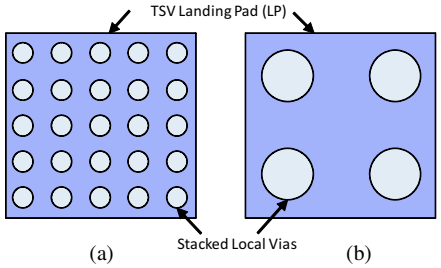


Fig. 11. Example of trade-off between the size and the number of local vias. (a) has large number of small-sized local vias on top of the TSV landing pad, while (b) has small number of large-sized local vias.

explore the impact of this trade-off between size of local vias[3] (subject to via layer) and the number of vias connected to a TSV landing pad on the failure time from EM.

In our study of this trade-off, the diameter of vias d_{via} and the space between vias follows 45nm design rule [16]. These parameters from design rule give us the maximum number of vias within 3.6um×3.6um landing pad. Then the maximum current density of each local via $j_{o,via}$ is

$$j_{o,via} = \frac{I_{o,TSV}}{n \times A_{via}} = \frac{j_{o,TSV} \times A_{TSV}}{n \times A_{via}}, \tag{9}$$

where $I_{o,TSV}$ and $j_{o,TSV}$ are total current and current density of TSV, n is number of local via, and A_{via} is area of local via. We show $j_{o,via}$ of each layer in the third column of Table VI. Although V_1 is much smaller than V_8, up to 676 V_1 vias can be packed in a landing pad while 16 vias can in V_8, and current density of each local via does not show significant difference.

In the Table VI, *Init.* r_{void} and *Crit.* r_{void} represent the radius of an initial and critical void at the local via. We estimate the failure time of the MSV by our model as appeared in the seventh column of the Table. *Area* is the area occupied by n local vias at the via layer, and *Block Area* indicates the potential area penalty that includes area occupied by TSV when the TSV landing pad is located at the metal layer higher than M_1. Area and block area are defined as,

$$\text{Area} = n \times A_{via} \tag{10a}$$

$$\text{Block Area} = n \times A_{via} + (i_{VL} - 1) \times A_{TSV}, \tag{10b}$$

where n is number of local vias, and i_{VL} is via layer number (i.e. 1 for V_1, and 4 for V_4). From the seventh column of Table VI, we can see that failure time (Tf) improves as the via layer is located in the higher metal layer. This is mainly due to the larger critical void size to reach the failure criterion, and also due to the lower current density in V_4 and V_8.

In the last two columns, we show failure time per via area. Although Tf *per Area* for V_8 shows better robustness than V_1, if we consider all the blockage area occupied by TSV up to M_7, Tf *per Block Area* of V_8 becomes shorter than V_1. In sum, vias in a higher metal (e.g. M_8) provides better robustness then M_1 vias, when we pack as much as vias on the landing pad. However, in terms of failure time vs. block area efficiency, higher metal layer is not as good as lower metal area if we consider the total blockage area that takes up the space of the TSV.

[3]Here we use the terminology *local via* as a via in the BEOL metal layers (V_1–V_9), to differ from the TSV.

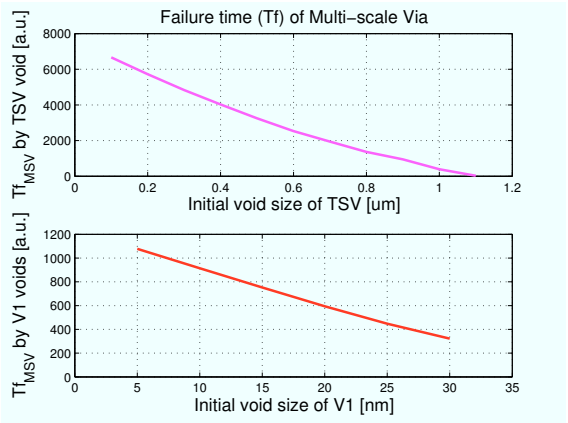


Fig. 12. Impact of initial void size on failure time of MSV; (Top) impact of TSV void size, when MSV failure time is driven by the TSV only, and (bottom) impact of V_1 void size, when MSV failure time is driven by the V_1s only.

E. Analysis on initial void size

In MSV, both TSV and local vias can have an initial void. First, TSV can have crack due to the thermo-mechanical stress generated by coefficient of thermal expansion (CTE) mismatch [19]. For local vias, as the feature size becomes smaller and the aspect ratio of the via trench increases, unsuccessful filling inevitably leaves nano-size voids, which grows with time [1]. Since the initial void size of TSV and local vias can affect the failure time of MSV, we examine how much impact they have through our EM model. First we reveal the impact of void size of TSV and local via (V_1) on failure time of MSV. Top figure of Figure 12 shows the impact of TSV void size on failure time, when only TSV is responsible to the failure time of MSV. Bottom figure describes impacts of local void size on failure time, when lifetime of MSV is driven by void growth of local vias only. As the initial void size increases, both cases show degraded robustness by having shorter lifetime, because it is easier to reach the critical void size with a large initial void.

In general, if only a TSV void governs failure time of MSV (top figure), it is more robust than the opposite case driven by local via voids only (bottom figure). However, we find out that if the TSV has very a large initial void, and V_1 has a smaller initial void, TSV void can dominate the MSV failure time even if both TSV and local vias have growing voids. The relationship between TSV initial void size and failure time of MSV is shown in Figure 13. In the figure, red line represents that only the TSV void grows and V_1 does not have any void; in green line, only the V_1 voids grow with fixed initial void (5nm); and in blue dotted line, both TSV and V_1 voids grow, with V_1 initial void as $5nm$. We can see that if the diameter of a TSV initial void is larger than 0.9um and that of a local via void is 5nm, and both TSV void and local via voids grow due to EM, it follows TSV void induced failure trends. Although 0.9um of TSV initial void seems to be an extreme case, it implies that TSV crack can have visible impact on the EM robustness of a MSV.

TABLE VI
TRADE-OFF BETWEEN THE SIZE OF VIA WITH DIFFERENT VIA LAYERS (V_1–V_8) AND THE NUMBER OF LOCAL VIAS. VIA SIZE IS BASED ON 45NM TECHNOLOGY [16].

Via Layer	d_{via}/ Space	# via / LP	$j_{o,via}$	Init. r_{void}	Crit. r_{void}	Tf [hrs]	Area [um^2]	Block Area[um^2]	Tf / Area	Tf / Block Area
V_1	65/75 nm	676	6.47MA/cm^2	5 nm	36.8 nm	1078	1.61	1.61	670 (1)	670 (1)
V_2	70/85 nm	529	6.95MA/cm^2	5 nm	38.0 nm	1044	1.50	5.65	696 (1.03)	185 (0.27)
V_4	140/160 nm	144	5.44MA/cm^2	5 nm	64.8 nm	2411	1.91	14.37	1261 (1.88)	168 (0.25)
V_8	400/440 nm	16	5.44MA/cm^2	5 nm	144 nm	5583	1.91	31.0	2923 (4.36)	180 (0.27)

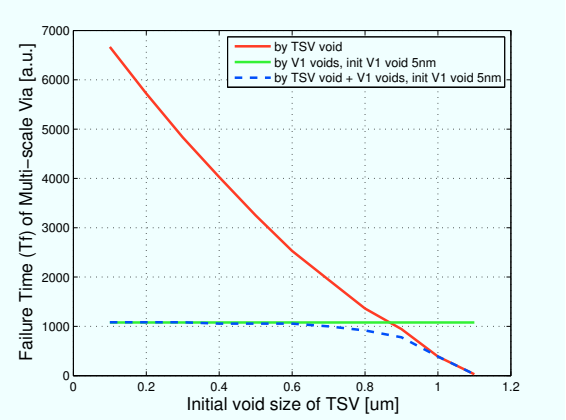


Fig. 13. Impact of a large void (crack) of TSV on failure time of MSV via structure. If a TSV initial void is larger than 0.9um and a local via void is 5nm, and both the TSV void and the local via voids grow due to EM, it follows TSV void induced failure trends.

V. SUMMARY AND CONCLUSION

In this work, we propose an efficient EM modeling flow for multi-scale via (MSV) structure in 3D PDN. Our experimental results show that EM modeling approaches only for TSVs or those for local vias may not be able to estimate the EM reliability of entire MSV, and that our integrated EM modeling approach is essential for MSV structures in 3D PDN.

We also investigate the impact of structure, material, and pre-existing void condition on EM-critical time of MSV of 3D PDN. For the material impact on the EM-induced failure time of MSV, we show that barrier resistivity can have significant effect on the lifetime of MSV. Also, enough local vias are shown to be necessary to achieve robustness of the MSV structure.

Out of the trade-off space between local via size and the number of local vias in MSV, we find that a small number of large vias can be preferable to many small vias in terms of EM. However, large vias on upper metal layers may have disadvantages of more blockage area for routing.

Finally, we find that barrier resistivity and pre-existing void condition can play a great role in EM lifetime of MSV structure. Depending on the pre-existing void condition, the lifetime of MSV can be dominated by either TSV or the local via array. In many cases, EM reliability is more likely to be dependent on local vias than TSV. However, if we have local vias without voids, or the pre-existing void of the TSV is large enough, EM of TSV can also dominate the failure time of MSV.

Based on this work, we will further investigate EM of full-chip level 3D PDN, with IR-drop analysis. We also believe consideration of grain distribution, mechanical stress effect, and statistical nucleation time analysis can further enhance the accuracy of EM estimation.

ACKNOWLEDGMENT

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