Adding the Missing Time-Dependent Layout Dependency into Device-Circuit-Layout Co-Optimization

—*New Findings on the Layout Dependent Aging Effects*

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Abstract

In this paper, a new class of layout dependent effects (LDE)—the *time-dependent* layout dependency due to device aging, is reported for the first time. The BTI and HCI degradation in nanoscale HKMG devices are experimentally found to be sensitive to layout configurations, even biased at the same stress condition. This new effect of layout dependent aging (LDA) can significantly mess the circuit design, which conventionally only includes the static LDE modeled for time-zero performance. Further studies at circuit level indicate that, for resilient device-circuit-layout co-design, especially to ensure enough design margin near the end of life, LDA cannot be neglected. The results are helpful to guide the cross-layer technology/design co-optimization.

Introduction

In advanced technology nodes, layout dependent effects (LDE) have been paid growing attention, which induce additional device variability and circuit design challenges [1-4]. Although extensive studies have been reported for static LDE on time-zero device performance, little information is available so far on the time-dependent LDE, especially when considering end-of-life (EOL) behaviors, which is particularly more important because near the end of life, the design margin will be shaved away due to transistor aging [5-8]. Thus, the investigation on layout dependency of aging emerges as an urgent demand for the resilient technology/design co-optimization against LDE during circuit aging. However, to our best knowledge, there has been no report on this issue yet.

In this paper, the layout dependency of device aging is experimentally studied for the first time in nanoscale high-κ/metal-gate (HKMG) technology. Underlying physical mechanisms are discussed in detail. With the further analysis at circuit level, the layout dependent aging (LDA) effects towards device-circuit-layout co-optimization are investigated.

Devices and Characterization Method

Devices of different layout designs with advanced HKMG gate stack are used in this work (Fig. 1). As shown in Fig. 2, typical LDE can affect the time-zero device performances. The variations of length of diffusion (LOD) and oxide spacing (OSE) impact the device mobility by altering the conductivity effective mass and intervalley phonon scattering due to variations of strain [9], while metal boundary effect (MBE) mainly affects the threshold voltage V_{th} due to the metal diffusion at the N/P boundary [4]. To characterize the layout dependency of device aging, ultra-fast "stress-sense-stress" technique is adopted to eliminate the recovery of BTI (Fig. 3(a)). When applying HCI stress to nFETs, the resulted degradation will consist of HCI and PBTI components [10], as shown in Fig. 3(c).

Experimental Results and Discussion

A. Layout Dependent NBTI in pFETs

As shown in Fig. 4 and 5, the V_{th} degradation (ΔV_{th}) of pFETs under NBTI stress increases with the decrease of S/D length (*SA*) and oxide definition spacing (*ODS*), indicating worse NBTI reliability with pitch scaling. While for MBE, ΔV_{th} decreases with the closer proximity of N/P boundary (*SPM*) (Fig. 6), which is reverse to the trend of V_{th} (Fig. 2(c)). The superimposed impacts of the three LDE to NBTI are illustrated in Fig. 7. Besides LOD, extra impacts of MBE and OSE, induced by N/P boundary and STI between neighboring devices in practical circuit layout respectively, will accelerate device degradation.

The NBTI degradation is directly correlated with the energy distributions of oxide traps [11]. As shown in Fig. 8, the extracted trap energy density with the method in [6, 12] increases with the decrease of *SA* and *ODS*, indicating that LOD and OSE affect the hole trapping in the gate oxide. However, the trap energy density decreases with reducing *SPM*, which could be due to the elimination of defects in pFETs by the nitrogen species diffused from the TiN gate of nFETs [13]. The measured *1/f* noise can further verify the trends of oxide trap energy density (Fig. 9&10). The impact of LOD and OSE on oxide hole trapping behaviors originates from hole capture barrier and tunneling probability. The compressive strain in pFETs induced by embedded SiGe S/D will lead to the shift of valence band [9], as well as changes of out-of-plane mass by band warping [14]. Since the resulted strain decreases with reducing *SA*, the up-shift of heavy hole band and out-of-plane effective mass will decrease, which will worsen the NBTI reliability due to the reduced hole capture barrier (Fig. 11) and increased tunneling probability according to the multi-phonon assisted trapping theory [11]. On the other hand, STI will induce tensile strain in the channel by using the high aspect ratio process (HARP) [15]. With the decrease of *ODS*, the induced tensile strain will increase, resulting in the decrease of effective compressive strain in the

channel. Therefore, the NBTI reliability will become worse due to the changes of valence band discussed above. The measured activation energy (Fig. 12) and gate tunneling current (Fig. 13) with varying *SA* and *ODS* also verify the proposed physical mechanisms.

B. Layout Dependent HCI&PBTI in nFETs

As shown in Fig. 14, the ΔV_{th} of LOD nFETs under HCI stress increases with the decrease of *SA*, indicating worse HCI&PBTI reliability as well. Since HCI&PBTI are correlated with the energy distributions of interface states and oxide traps, the trap energy densities before and after HCI stress are extracted as shown in Fig. 15(a)&(b). The net trapped charge density (Fig. 15(c)) increases with decreasing the *SA*, which is due to the impacts of LOD on electron trapping. The tensile strain in nFETs will lead to the splitting of conduction bands into Δ2 and Δ4 bands [9]. With the decrease of *SA*, the down-shift of Δ2 and out-of-plane effective mass will decrease due to the reduced strain. This will result in a lower electron capture barrier and larger tunneling probability (Fig. 16), and thus worsen HCI&PBTI. The trend of the measured effective activation energy (Fig. 17) and gate tunneling current (Fig. 18) can also verify the analysis above.

As shown in Fig. 19, the HCI&PBTI of OSE nFETs become worse with the decrease of *ODS*. The extracted trap energy densities before and after HCI stress as well as the net trapped charge density manifest increasing trends with the decrease of *ODS* (Fig. 20). Since STI with HARP induces tensile strain, the effective tensile strain in the channel of nFETs will increase with reducing *ODS*, resulting in the increase of mobility (Fig. 2(b)) and weakened Si-H bonds. As a result, the HCI&PBTI will become worse due to more severe defects generation with decreasing *ODS*, consistent with the smaller effective activation energy shown in Fig. 21.

Towards Device-Circuit-Layout Co-Optimization with LDA

Based on the above results, the time-dependent LDE are added to the device-circuit-layout co-optimization with the developed compact model, in addition to the time-zero LDE and post-layout parasitics (R&C) (Fig. 22). INV and NAND2 gates from different standard cell libraries are simulated for demonstrations (Fig. 23). The competing dependences of aging on *SA*, *ODS* and *SPM* will complicate the device-circuit-layout co-design, causing the end-of-life (EOL) circuit performance sensitive to layout configurations. As shown in Fig. 24, compared with conventional layout independent aging (LIA), EOL delay & power of most layout configurations of the inverter increase with considering LDA; while other layout configurations manifest decreasing trend. This will induce remarkable errors in predicting the circuit EOL performance. As an example, nominal EOL delay of some layout configurations of the inverter can be under-estimated by as large as 11.5% if w/o considering LDA. Compared with the 10% failure criterion in circuit reliability assessment, these deviations are intolerable, which will further increase at high-sigma tails if adding the process and dynamic variability [6]. From the perspective of circuit optimization, the EOL metric PPA (power/performance/area) [16] of inverter changes greatly between LIA and LDA (Fig. 25), especially the area of the optimal layout targeting below specific EOL power and delay can be under-estimated by 38% with LIA (Fig. 26). For the layout optimization against LDE, sensitivity analysis is carried out for LOD, OSE and MBE. As shown in Fig. 27, the EOL delay of inverters is most sensitive to MBE, which manifests non-monotonic dependency on *SPM* due to the competing impacts from parasitics, static LDE and LDA (Fig. 22). Thus the N/P boundary proximity effect should be paid more attention in nanoscale HKMG technology. Similar results are obtained regarding the impacts of LDA on NAND2 gates (Fig. 28). Therefore, aiming to guarantee enough design margin near end of life, the LDA cannot be neglected. By comprehensive device level characterization and modeling, the layout dependency of aging should be incorporated into the post-layout simulation for reasonable device-circuit-layout co-optimization.

Summary

We have experimentally studied the missing layout dependency of device aging effects for the first time in nanoscale HKMG technology. Evident layout dependences of BTI and HCI reliability are observed with the detailed discussion on the underlying physics. The complex layout dependency of device aging sheds light on the necessity of adding LDA into the reliability-aware circuit design. With further analysis at the circuit level, large deviations of circuit PPA will be introduced between LIA and LDA, indicating that layout dependency of aging cannot be neglected in the device-circuit-layout co-optimization. The results in this work are helpful for the cross-layer technology/design co-optimization at nanoscale nodes.

Acknowledgement

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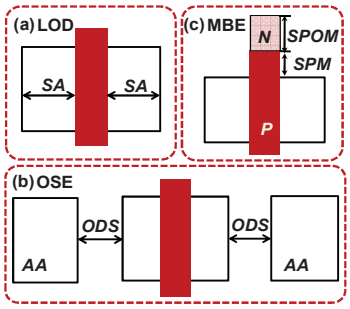

Fig. 1 Illustrations of three typical layout dependent effects studied in this work, (a) length of diffusion effect (LOD), (b) OD to OD spacing effect (OSE) and (c) metal boudary effect (MBE).

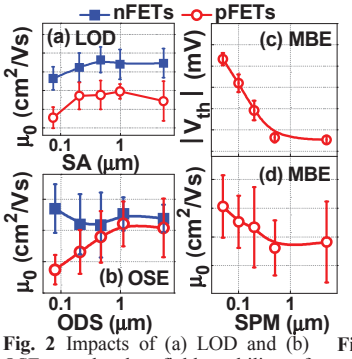

Fig. 2 Impacts of (a) LOD and (b) OSE on the low-field mobility of nFETs and pFETs. Impacts of MBE on the (c) threshold voltage V_{th} and (d) low-field mobility of pFETs.

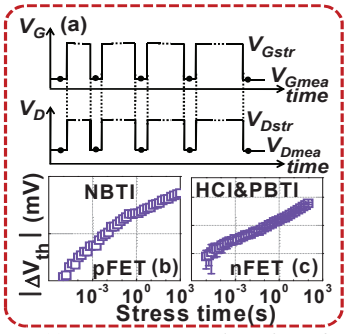

Fig. 3 (a) Measurement schematics of ultra-fast "stress-sense-stress" technique with 5μs sensing time used in this work. For NBTI, the drain voltage is set as 0 during stress and V_{Dmea} during sensing. Typical results of (b) NBTI for pFETs and (c) HCI&PBTI for nFETs.

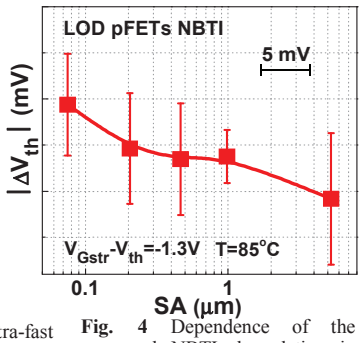

Fig. 4 Dependence of the measured NBTI degradation in pFETs with LOD design (LOD pFETs) on the S/D length (*SA*). With the decrease of *SA*, NBTI degradation worsens.

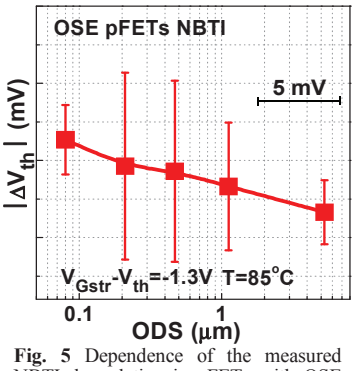

Fig. 5 Dependence of the measured NBTI degradation in pFETs with OSE design (OSE pFETs) on the oxide definition spacing (*ODS*). With the decrease of *ODS*, larger NBTI degradation can be oberserved.

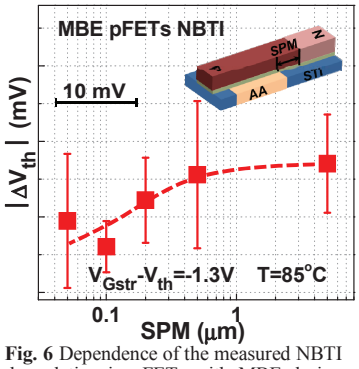

Fig. 6 Dependence of the measured NBTI degradation in pFETs with MBE design (MBE pFETs) on the proximity of N/P boundary (*SPM*). With the decrease of *SPM*, the NBTI degradation will be reduced.

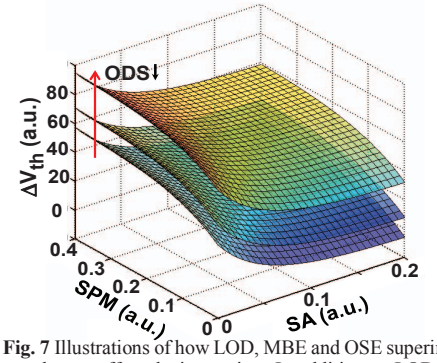

Fig. 7 Illustrations of how LOD, MBE and OSE superimpose together to affect devices aging. In addition to LOD, extra impacts of MBE from N/P boundary, and OSE from STI between neighboring devices in practical circuit layout, will accelerate the device degradation.

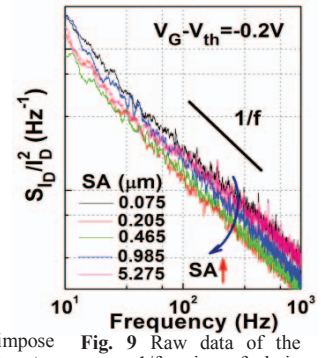

Fig. 9 Raw data of the mean 1/f noise of drain current with varying *SA* in pFETs under V_G-V_{th}=-0.2V and V_D=-50mV.

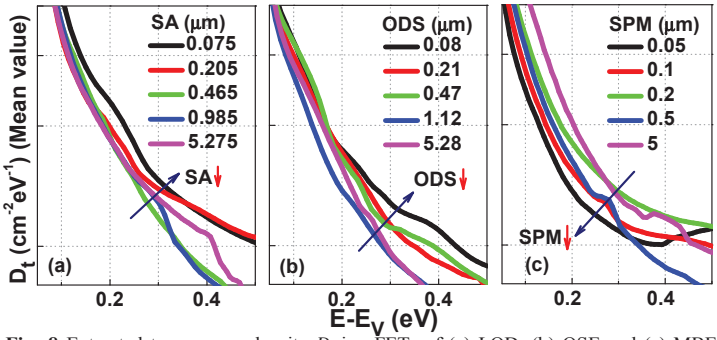

Fig. 8 Extracted trap energy density D_t in pFETs of (a) LOD, (b) OSE and (c) MBE design with varying *SA*, *ODS* and *SPM* respectively. Every curve is the mean value of multiple devices with the same size. It can be found that the trends of D_t with varying *SA*, *ODS* and *SPM* are consistent with those of ΔV_{th}. Therefore, LDE will affect the hole trapping behaviors in the gate oxide during NBTI stress.

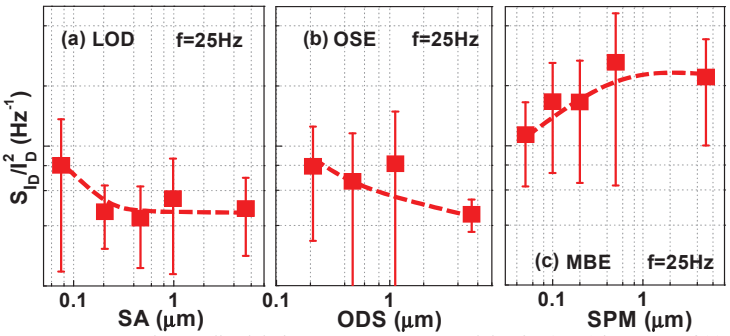

Fig. 10 Extracted normalized drain current power spectral density (PSD) in pFETs of (a) LOD, (b) OSE and (c) MBE design with varying *SA*, *ODS* and *SPM* respectively. Since drain current 1/f noise is induced by trapping/detrapping effect in the gate oxide, the trends of normalized PSD can reflect the magnitude of oxide trap density, which are consistent with the extracted trap energy density in Fig. 8.

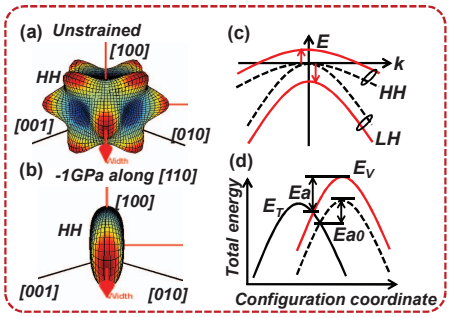

Fig. 11 Heavy hole band equi-energy contours calculated using MASTAR [17] under (a) unstrained condition and (b) 1GPa compressive strain along [110]. (c) Energy splitting of heavy hole (HH) band and light hole (LH) band when strain is applied. (d) Impact of energy splitting on hole capture barrier in configuration coordinate diagram.

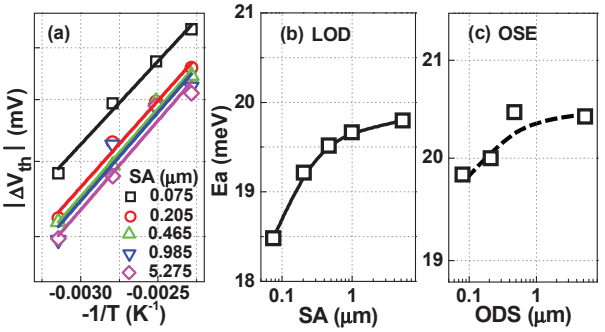

Fig. 12 (a) Temperature dependence of $|\Delta V_{th}|$ in pFETs of LOD design with varying *SA*, which manifests thermal activation characteristics. (b) Extracted activation energy *Ea* with varying *SA* in pFETs of LOD design. (c) Extracted activation energy *Ea* with varying *ODS* in pFETs of OSE design. Clear dependences of *Ea* on *SA* and *ODS* can be observed.

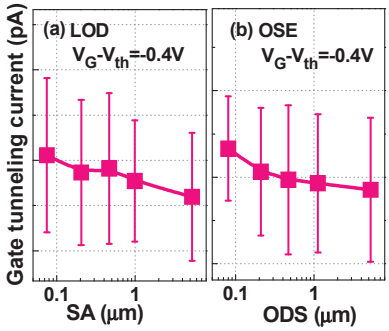

Fig. 13 Measured gate tunneling current in pFETs of (a) LOD and (b) OSE design with varying *SA* and *ODS* respectively. It can be observed that the trends of gate tunneling current are consistent with those of out-of-plane effective mass and tunneling barrier induced by strain.

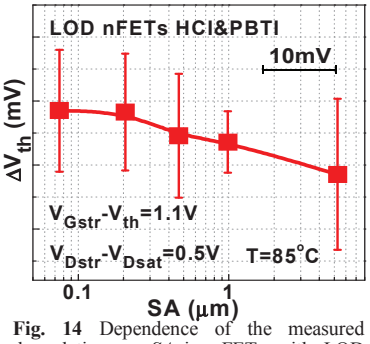

Fig. 14 Dependence of the measured degradation on *SA* in nFETs with LOD design (LOD nFETs) under HCI stress. ΔV_{th} increases with the decrease of *SA*. It should be noted that the total degradation consists of HCI and PBTI components.

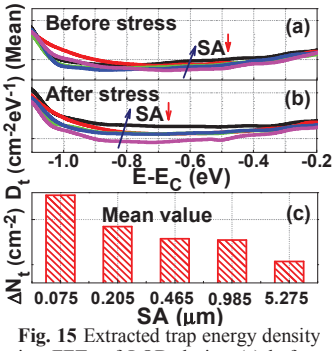

Fig. 15 Extracted trap energy density in nFETs of LOD design (a) before and (b) after HCI stress. (c) Extracted net trapped charge density generated during HCI stress with varying *SA*.

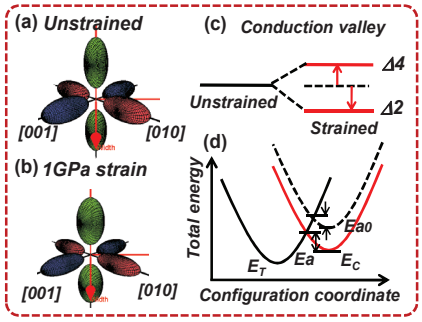

Fig. 16 Equi-energy contours of conduction band electrons calculated using MASTAR [17] under (a) unstrained condition and (b) 1GPa tensile strain along [110]. (c) Energy splitting when stain is applied. (d) Impact of energy splitting on electron capture barrier in configuration coordinate diagram.

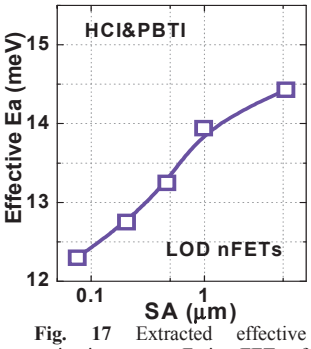

Fig. 17 Extracted effective activation energy *Ea* in nFETs of LOD design (LOD nFETs) under HCI stress with varying *SA*. Clear dependence of *Ea* on *SA* can be observed.

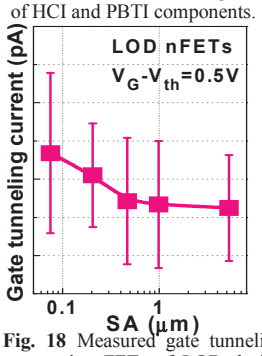

Fig. 18 Measured gate tunneling current in nFETs of LOD design (LOD nFETs) with varying *SA*. The trend of gate tunneling current is consistent with those of out-of-plane effective mass and tunneling barrier induced by strain.

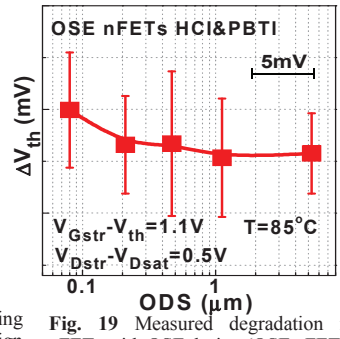

Fig. 19 Measured degradation in nFETs with OSE design (OSE nFETs) under HCI stress with varying *ODS*. ΔV_{th} increases with the decrease of *ODS*. It should be noted that the total degradation consists of HCI and PBTI components.

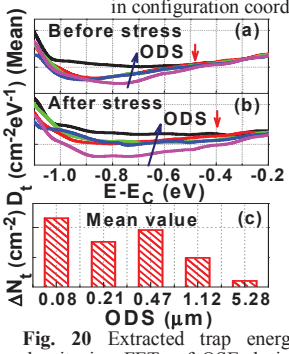

Fig. 20 Extracted trap energy density in nFETs of OSE design (a) before and (b) after HCI stress. (c) Extracted net trapped charge density generated during HCI stress with varying *ODS*.

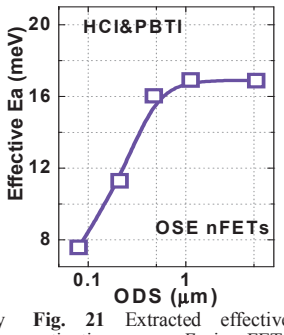

Fig. 21 Extracted effective activation energy *Ea* in nFETs of OSE design (OSE nFETs) under HCI stress with varying *ODS*. Clear dependence of *Ea* on *ODS* can be observed.

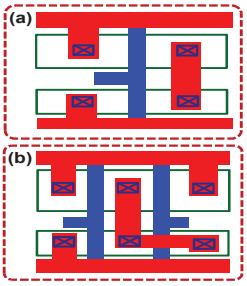

Fig. 23 Layouts of the demonstrated circuits in this work: (a) INV and (b) NAND2 gates. More than 200 types of layout with different sizes (i.e. *SA*, *ODS*, *SPM*) are studied for each circuit.

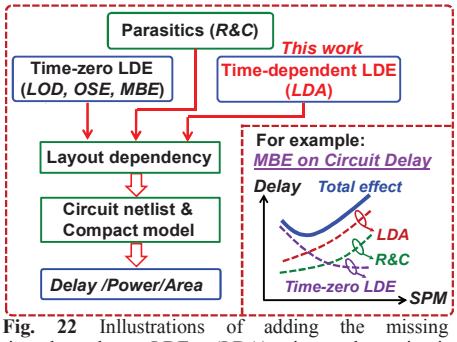

Fig. 22 Illustrations of adding the missing time-dependent LDE (LDA) into the circuit performance prediction besides the time-zero LDE and parasitics (R&C). Taking MBE as an example, the competing impacts from R&C, time-zero LDE and LDA result in the non-monotonic trend of delay with varying *SPM*.

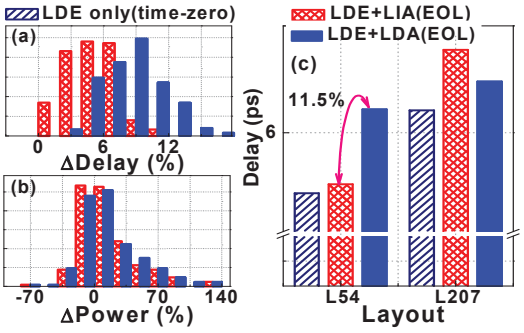

Fig. 24 The distributions of (a) Δdelay ($delay_{EOL}$-$delay_{fresh}$) and (b) Δpower ($power_{EOL}$-$power_{fresh}$) considering EOL layout independent aging effects (LIA) and EOL layout dependent aging effects (LDA) normalized to time-zero inverter with LDE only. (c) Delay of two typical layouts (*Layout 54*, *Layout 207*) of inverter considering LDE only (time-zero), LDE+LIA (EOL) and LDE+LDA (EOL) respectively.

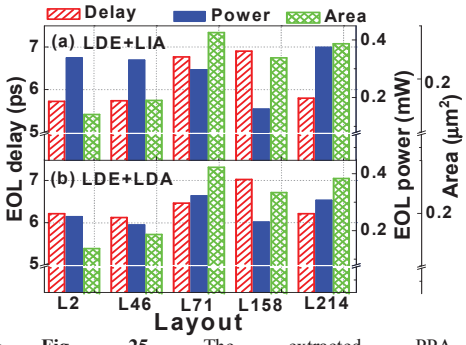

Fig. 25 The extracted PPA (performance/power/area) near end of life for five inverter layouts (*Layout 2*, *Layout 46*, *Layout 71*, *Layout 158*, *Layout 214*) w/ (a) LDE on time-zero device performance & LIA (EOL) and (b) LDE on time-zero device performance & LDA (EOL). Significant deviations can be observed.

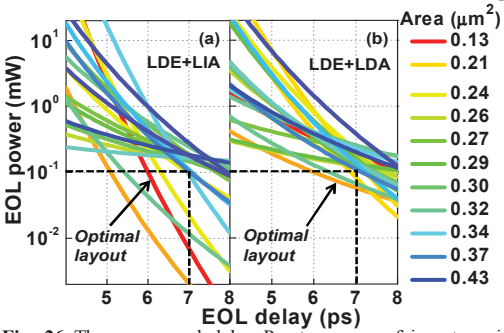

Fig. 26 The power and delay Pareto curves of inverter with varying layout areas considering (a) LDE on time-zero device performance and EOL layout independent aging (LIA), (b) LDE time-zero device performance and EOL layout dependent aging (LDA). Constained to power<0.1mW and delay<7ps, the area of the optimal layout will be under-estimated by 38% with LIA.

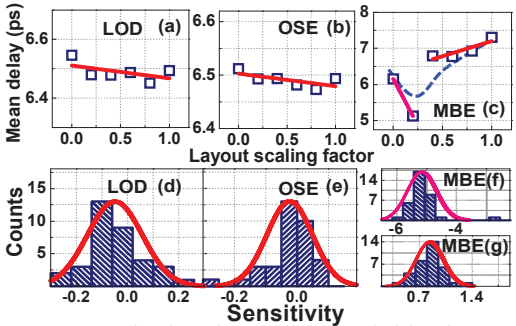

Fig. 27 The dependences of averaged delay for inverter near end of life on layout scaling factor of (a) LOD, (b) OSE and (c) MBE. The distributions of the sensitivity of EOL delay to (d) LOD, (e) OSE, (f) MBE for negative trend and (g) MBE for positive trend which are explaied in Fig. 22.

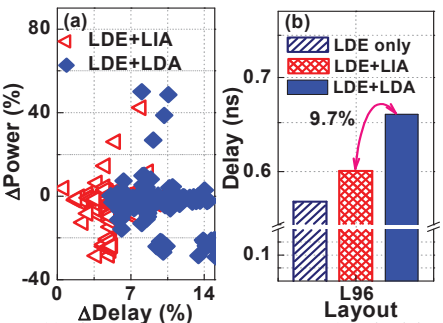

Fig. 28 (a) The Δpower ($power_{EOL}$-$power_{fresh}$) and Δdelay ($delay_{EOL}$-$delay_{fresh}$) considering EOL LIA and EOL LDA normalized to time-zero NAND2 with staic LDE only. (b) Delay of typical layout of NAND2 considering LDE only, LDE+LIA (EOL) and LDE+LDA (EOL) respectively.The resulted deviation of 9.7% is close to the failure criterion of 10% in reliability assessment.