Table 2: Insertion Rate (IR) Comparison

Bench	#Vias	Un-constrained	SP-ILP	DP-ILP	DP-Ap	TP-ILP	TP-Ap
efc	4983	98.45	75.15	98.29	96.84	98.41	97.89
ecc	5523	99.02	78.68	98.80	97.44	98.98	98.62
ffu	7026	98.57	76.77	98.47	97.35	98.54	97.93
alu	7046	98.32	72.79	98.15	96.39	98.29	97.44
byp	28847	93.88	70.21	N/A	91.35	N/A	92.88
mul	62989	98.55	68.59	N/A	94.91	N/A	96.86
Avg.	19402	97.80	73.70	N/A	95.71	N/A	96.94

redundant via insertion with multiple patterning simultaneously. To improve scalability, we propose an approximation algorithm with LP relaxation and rounding to solve the problem efficiently. The experimental results demonstrate that our methods can insert redundant via with the consideration of DSA guiding template shapes without much loss of insertion rate. Our methods can be adaptive to different technology nodes as well.

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