A Scaling Compatible, Synthesis Friendly VCO-based Delta-sigma ADC Design and Synthesis Methodology

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ABSTRACT

Conventional analog/mixed-signal (AMS) circuits design methodology relying heavily on the use of operational amplifiers (opamps) to process signals in voltage-domain (VD) encounters severe difficulties in advanced nanometer-scale CMOS process. We present a novel scaling compatible, synthesis friendly ring voltage-controlled oscillator (VCO) based time-domain (TD) delta-sigma analog-to-digital converter (ADC) whose performance improves as technology advances. Decomposed into digital gates (e.g. inverters) and a small set of simple customized cells (e.g. resistors), its layout is fully synthesizable by leveraging digital layout synthesis tools. Post-layout simulation results demonstrate the scaling compatibility of the proposed ADC and a drastic boost to design productivity.

1. INTRODUCTION

The conventional way to design analog/mixed-signal (AMS) circuits relies heavily on the use of operational amplifiers (opamps) to process signals in the voltage domain (VD). The well-established VD AMS design methodology encounters severe difficulties in advanced nanometer-scale CMOS process due to reduced supply voltages and transistor intrinsic gains. For instance, as the transistor feature size shrinks from 0.5um to 22nm, the transistor intrinsic gain drops from 180 to 6, and the supply voltage decreases from 5V to 1V (see Fig. 1a) [1]. Conventional VD-AMS architectures depend on the high gain of opamps to guarantee precision and linearity; however, the required high gain is very difficult to achieve with a small transistor intrinsic gain. A low supply voltage further increases the difficulty, as it prevents the use of many gain boosting techniques that require stacking transistors vertically. Hence, long-channel thick-oxide transistors and high supply voltages have to be used for VD-AMS, resulting in limited performance enhancement and area/cost reduction as technology advances, in contrast to their digital counterparts.

The advent of nanometer CMOS technology calls for a new AMS framework that not only does not suffer from scaling but actually benefits from it. As shown in Fig. 1b, one clear merit of CMOS scaling is that the transistor speed, as characterized by f_T, has increased from 16 GHz at 0.5um to 400 GHz at 22nm. The timing resolution, as represented by the fan-out-of-4 (FO4) delay of an inverter, has also improved from 140ps to 6ps. As a result, it is promising to process analog information in the time domain (TD) or phase domain instead of in VD, leading to the concept of TD-AMS. TD-AMS framework has been adopted among a wide range of AMS circuits [2–7]. They care less about VD accuracy, obviating the need for opamps. The integration in the phase domain is performed by a ring voltage-controlled oscillator (VCO), and the phase comparison can be realized using an XOR gate. They are area/power efficient, operate well under low voltage, and their performance improves as the inverter delay decreases and the timing resolution increases with the advance in process technology. Therefore, TD-AMS is a promising scheme which enjoys superb *scaling compatibility*.

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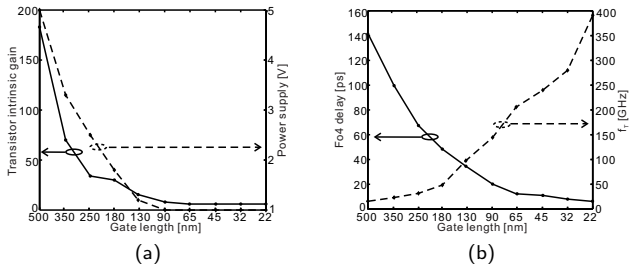


Figure 1: (a) Power supply and transistor intrinsic gain scaling trend. (b) f_T and FO4 delay trend.

In addition to the challenge posed by CMOS scaling, another key limitation for conventional AMS circuit design is low productivity. Although much progress has been made by electronic design automation (EDA) researchers on the automatic layout synthesis for AMS circuits [8–14], the tools are still immature and have not been widely used in practice. The majority of the AMS layout design efforts are still handled manually. Recently, some early attempts (including ADCs [15–17], phase-locked loop (PLL) [18], filters [19]) have been made to design AMS circuits to be digital-like and reasonably robust to layout effects (e.g. mismatches), so that they can be described in Hardware Description Languages (HDLs) and synthesized using digital layout synthesis tools. Such *synthesis friendly* AMS circuit design and synthesis methodology greatly improves design productivity and reliability, reduces design cost, as well as shortens product turn-around time and time-to-market compared with the conventional AMS circuit design flow (see Fig. 2). This is because not only the layout synthesis becomes substantially easier, but describing AMS circuit in HDL also greatly enhances circuit portability.

Ultra-low-power and ultra-low-voltage ADCs compatible with CMOS scaling are in increasingly high demand by emerging applications, including internet-of-things (IoT), autonomous wireless sensor networks (WSN), and biomedical implants. While the ADCs presented in [15–17] are fully digitally synthesizable, they did not achieve desirable circuit performances (e.g. Walden figure-of-merit (FOM) [20], signal-to-noise and distortion ratio (SNDR)) nor demonstrate scalability. In this paper, for the first time, we present a novel scaling compatible, synthesis friendly TD VCO-based continuous-time (CT) delta-sigma ($\Delta\Sigma$) ADC whose

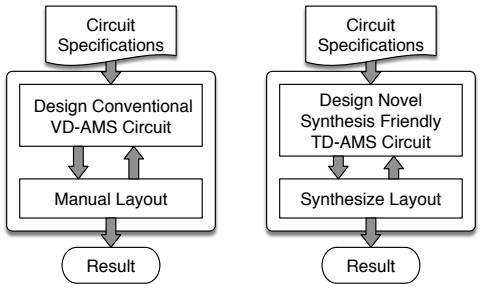


Figure 2: (a) Conventional VD-AMS circuits design flow. (b) Novel synthesis friendly TD-AMS circuits design flow.

performance improves as technology advances. Decomposed into digital gates (e.g. inverters) and a small set of simple customized cells (e.g. resistors), its layout is fully synthesizable by leveraging digital layout synthesis tools. Our main contributions are summarized as follows:

- This is the first work to design a highly scaling compatible TD VCO-based CT $\Delta\Sigma$ ADC to be fully synthesis friendly;
- A significant productivity improvement to AMS circuit layout is obtained with our proposed design and synthesis methodology;
- Our circuit performance compares favorably with previous works on synthesis friendly ADC design, and excellent scaling compatibility is demonstrated.

The rest of this paper is organized as follows: Section 2 gives the complete circuit design of the scaling compatible, synthesis friendly VCO-based $\Delta\Sigma$ ADC. Section 3 presents the layout synthesis methodology for our designed circuit. Section 4 shows the experimental results. Finally, Section 5 concludes the paper.

2. CIRCUIT DESIGN

2.1 Basics of Delta-sigma ADC

The block diagram of a $\Delta\Sigma$ ADC is shown in Fig. 3. By placing the quantizer in a feedback loop that contains a high-gain, low-pass loop filter, the quantization error appears at the output can be high-pass shaped. With subsequent low pass filtering and decimating in digital domain, the effect of quantization to the in-band signal can be suppressed. Therefore, $\Delta\Sigma$ ADC facilitates us to use a low resolution, easy-to-build quantizer to achieve high resolution conversion. This type of ADC is an important building block for many mobile, audio and radar applications.

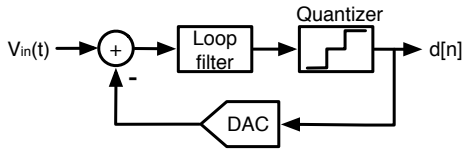


Figure 3: Block diagram of a $\Delta\Sigma$ ADC.

2.2 Proposed Synthesis Friendly Delta-sigma ADC

Fig. 4 shows the architecture of the proposed $\Delta\Sigma$ ADC. It is divided into slices, where the number of slices is selected according to the effective quantizer resolution requirement. Each slice can be decomposed into simple independent circuit building blocks, including an XOR gate, a digital-to-analog converter (DAC), retiming latches, ring VCOs, buffers, and comparators. The VCO stage which works as an integrator can be simply built by 4 cross-coupled inverters (see Fig. 5). The buffer, which is similar to the VCO stage except that it has a fixed bias tail, is used to isolate kickback noise [6]. The comparator samples the output of the replica buffer. Because of its simple structure, the proposed ADC allows easy adaptations to different specifications as long as they are within the ADC performance boundary in a given process. For example, to increase the effective quantizer resolution, we can simply add more slices. To widen the signal bandwidth, we can increase the clock frequency. To increase SQNR, we can boost the loop gain by increasing either the DAC feedback current or the VCO tuning gain. The ability to be decomposed into simple circuit building blocks (digital gates and resistors) facilitates the adoption of digital layout synthesis flow. Further detailed circuit analysis can be found in [5,6].

Besides synthesis friendliness, an additional benefit of the proposed ADC is its superb scaling compatibility. Firstly, it is robust against non-idealities, such as device parasitics and mismatches, which are major challenges in nanometer-scale CMOS process. Both the VCO mismatches and comparator offset are high-pass shaped, and thus, hardly affect ADC performance. Secondly, the timing resolution increases and the performance improves as the process technology advances, in light of the fact that the delay of the inverters in the VCO becomes shorter and shorter with CMOS scaling [1]. Moreover, the proposed ADC also operates well under low voltage. These factors have made it a favorable choice in the advanced CMOS process.

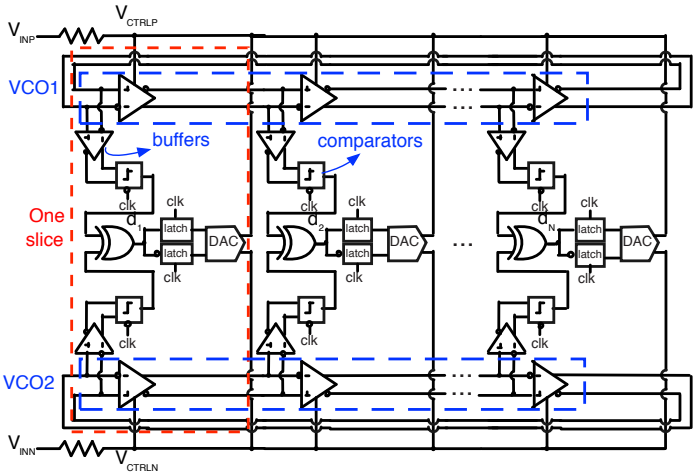


Figure 4: The proposed scaling compatible, synthesis friendly VCO-based $\Delta\Sigma$ ADC architecture.

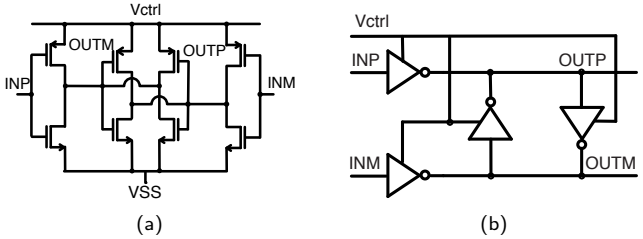


Figure 5: (a) Transistor level schematic of VCO cell. (b) VCO implemented using digital inverters gates.

2.2.1 *Novel Synthesis Friendly TD Analog Comparator Design*

As the VCO nodes switch with relatively low swing (e.g. 0.5V typically), the sense amplifier flip flops (SAFFs) used to latch the VCO outputs usually employs a strongARM comparator for robust latching as well as intrinsic level shifting. However, conventional strongARM comparators are classified as AMS circuit and thus not implemented in the standard cell library. To overcome this issue, [16] proposed to form a comparator with two cross-

coupled 3-input NAND gates, providing a synthesis friendly alternative of the strongARM comparator. This solution, however, requires the input common mode (CM) to be sufficiently high. In the proposed ADC, the input of the SAFF interfaces with the VCO buffer, whose output CM resides at around only 0.25V. For this reason, we proposed a modified comparator design using cross-coupled 3-input NOR (NOR3) gates, which easily facilitates low common mode input. The schematic of a PMOS input strongARM comparator and the proposed NOR3-based comparator are shown in Fig. 6a and Fig. 6b respectively. We can observe that the NOR3-based comparator resembles the former. Under 0.25V input CM, the NMOS pair marked in blue are essentially cut off, and thus the proposed comparator is functionally identical to the strongARM comparator. Noteworthily, as the TD nature of this ADC desensitized VD related non-idealities such as offset and memory effect, the default NOR3 layout can be used without special modification and imposing additional placement and routing (P&R) constraint.

The complete SAFF gate-level schematic is shown in Fig. 7. The SR-latch following the NOR3-based comparator provides logic keeping when the comparator resets.

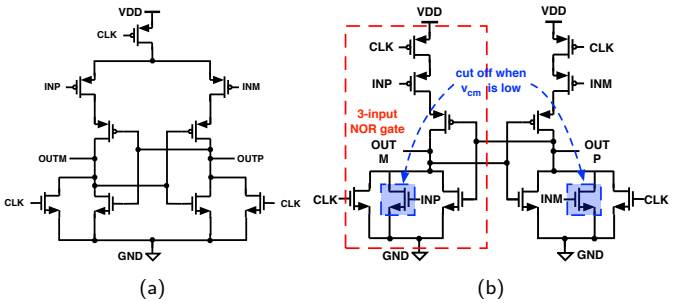


Figure 6: (a) Regular TD comparator. (b) TD comparator by connecting two 3-input NOR gates.

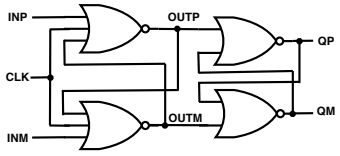


Figure 7: Proposed TD comparator gate-level implementation with SR-latch.

2.2.2 *Synthesis Friendly DAC Architecture Selection*

Synthesizable voltage DAC architecture using basic logic gates has been previously reported in [18]. Nevertheless, in CT $\Delta\Sigma$ ADC, current DACs are preferred as it simplifies the feedback network. An example schematic of a conventional current-steering DAC is shown in Fig. 8a. This structures is not readily available in the standard cell library. In addition, an analog intensive bias generation network is also required for this type of DAC. The bias network must be manually laid out to guarantee functionality and matching, thus making current-steering DAC highly synthesis unfriendly. In this work, we propose to use resistor DAC over conventional current-steering structure. To source current, we connect the resistor between the feedback point and V_{REFP}. To sink current, we connect the resistor between the feedback point and ground. This can be simply implemented by a resistor and an inverter, as illustrated in Fig. 8b. Hence, we only need to insert a simple cell into the library representing a resistor fragment and synthesize a DAC through proper instantiation. As resistors exhibit high raw matching and do not require bias, P&R requirements are also relaxed for resistor DAC.

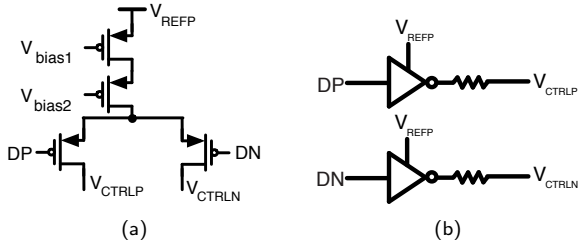


Figure 8: (a) A conventional current-steering DAC. (b) The resistor DAC used in our synthesis friendly ADC circuit.

3. SYNTHESIS METHODOLOGY

Previous synthesis friendly AMS circuit design works [15–19] adopted the digital automatic placement and routing (APR) flow to generate the layouts by turning off the optimizations that are irrelevant, including logic optimization, timing optimization, etc. However, this oversimplified paradigm shows its limitations when applied to the ADC circuit we design. The reason lies in that the power domains (PDs) and circuit components groups constraints were not incorporated into their flow while they are required in our circuit, which will be further discussed in Section 3.3. Hence, this calls for a layout synthesis methodology for synthesis friendly AMS circuit that is capable of handling PDs and components groups constraints, motivating our layout synthesis methodology.

Fig. 9 shows the overall flow of our approach. The HDL files generation phase, standard cell library modification phase, together with the floorplan generation phase prepares input data to the APR stage, which include the gate-level netlist in HDL (e.g. Verilog), files describing the modified standard cell library (e.g. LEF and GDSII files), as well as the floorplan specification (e.g. files with the .fp extension used in Cadence Encounter), respectively. APR is then performed to generate the final layout.

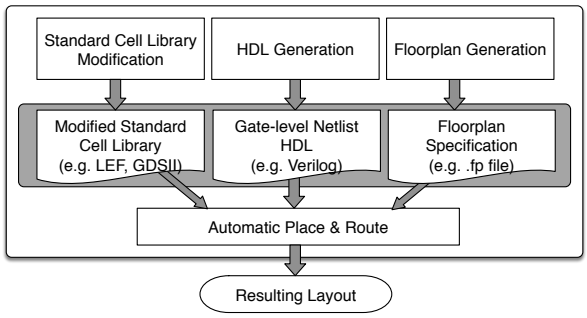


Figure 9: Over flow of the layout synthesis methodology for the proposed synthesis friendly ADC.

3.1 Standard Cell Library Modification

Standard cell library modification phase (see Fig. 10a) adds a small set of customized AMS circuit building blocks to the existing digital standard cell library. As discussed in Section 2, the only circuit building blocks that need to be customized are the resistors, while other building blocks can be implemented purely with digital gates. Each resistor is decomposed into several identical fragments and only the fragments are added to the standard cell library as special "standard cells", which we call *resistors standard cells*. High resistivity usually implies smaller area but lower accuracy, and smaller fragments often provide more placement flexibility while the routing may become more complicated. We design the resistors standard cells considering these trade-offs. Once the parameters of the resistors standard cells are determined, the layout of the resistors can be conveniently drawn from the foundry provided process design kit (PDK), requiring minimal manual design efforts.

Fig. 11 gives the layouts of the two customized resistors standard cells we generate using material with different resistivity. In the figure, the displayed dimensions of both resistors standard cells are scaled to have the same width so that both of them can be seen clearly. The actual heights of both resistors standard cells should be similar to the digital standard cell height. After that, we can export their layouts in GDSII format, merge them with the existing standard cell library, and generate the LEF and GDSII files describing the modified standard cell library.

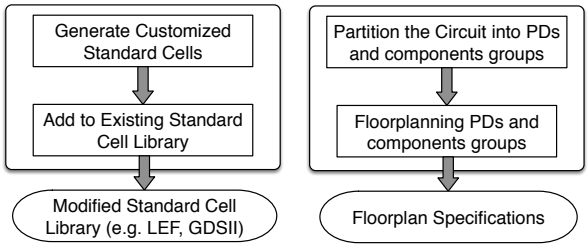


Figure 10: (a) Standard cell library modification. (b) Floorplan generation.

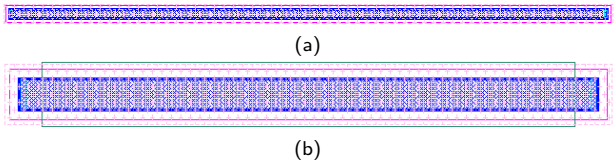


Figure 11: Generated resistors standard cells layouts: (a) 1kΩ resistor with lower resistivity. (b) 11kΩ resistor with higher resistivity.

3.2 HDL Generation

The HDL Generation phase converts the circuit netlist from schematic into a HDL representation. Since it is a common practice to design AMS circuits in schematic, our synthesis flow exports the circuit netlist designed in schematic into gate-level HDL (e.g. Verilog) using existing EDA tools (e.g. Cadence Virtuoso NC-Verilog). An added benefit is that being able to express the AMS circuit in HDL facilitates the AMS design porting between different technology nodes. Two example circuit modules of the designed synthesis friendly ADC in Verilog is given, with the Verilog description of the comparator circuit design shown in Table 1, and the top-level Verilog module of one slice of the ADC shown in Table 2. The resulting netlist is in gate-level instead of register-transfer level (RTL), because the logic synthesis methodologies designed for digital circuit may not be suitable for AMS circuit. Improper choices of standard cell sizes by the digital logic synthesis tools may destroy the AMS circuit functionality.

3.3 Floorplan Generation

In the proposed ADC circuit, there are several different Power/Ground (P/G) nets connected to the P/G pins of different standard cells. For example, the power pins of the inverters in VCO1 is connected to one of the VCO control nodes V_{CTRLP} (denoted as PD V_{CTRLP} in the figure), while the gates composing the comparator have their power pins connected to the VDD net (denoted as PD VDD). The entire circuit can be decomposed into several different PDs and groups. A power domain consists of the circuit components sharing the same power supply, while a components group is a group of circuit components that may not need power supply. Fig. 12 shows the PDs and components groups of one slice of the circuit. In conventional digital APR, the P/G rails of the cells in the same placement row will be connected and short their P/G pins, which will cause a problem if any two cells in the row are connected to different P/G nets.

Table 1: Example Verilog implementation of the proposed synthesis friendly comparator.

```
1  module comparator(Q,QB,VDD,VSS,CLK,INM,INP)
2  inout VDD, VSS;
3  input CLK, INM, INP;
4  output Q, QB;
5  wire OUTP, OUTM;
6  NOR3X4 I0 (.Y(OUTP), .VDD(VDD), .VSS(VSS),
               .A(OUTM), .B(INP), .C(CLK));
7  NOR3X4 I1 (.Y(OUTM), .VDD(VDD), .VSS(VSS),
               .A(OUTP), .B(INM), .C(CLK));
8  NOR2X1 I2 (.Y(Q), .VDD(VDD), .VSS(VSS),
               .A(OUTP), .B(QB));
9  NOR2X1 I3 (.Y(QB), .VDD(VDD), .VSS(VSS),
               .A(OUTM), .B(Q));
10 endmodule
```

Table 2: Example Verilog implementation of the proposed ADC slice.

```
1  module ADC_slice(CLK, IN, IN2, IP, IP2, ON, ON2,
   OP, OP2, VBUF, VCTRLN, VCTRLP, VDD, VREFP,
   VSS)
2  inout IN, IN2, IP, IP2, ON, ON2, OP, OP2, VBUF,
   VCTRLN,VCTRLP, VDD, VREFP, VSS;
3  input CLK;
4  wire BON, BOP, BON2, BOP2, DB, DAC_OUT,
   DAC_OUT_B;
5  buf_cell I0 (.BIN(ON), .BIP(OP), .BON(BON),
              .BOP(BOP), .VCTRL(VBUF), .VSS(VSS));
6  buf_cell I1 (.BIN(ON2), .BIP(OP2), .BON(BON2),
              .BOP(BOP2), .VCTRL(VBUF), .VSS(VSS));
7  pd_VDD I2 (.BON(BON), .BON2(BON2), .BOP(BOP),
              .BOP2(BOP2), .CLK(CLK), .D(DOUT),
              .DB(DB), .VDD(VDD), .VSS(VSS));
8  res_cell I3 (.T1(DAC_OUT_B), .T2(VCTRLN));
9  res_cell I4 (.T1(DAC_OUT), .T2(VCTRLP));
10 pd_VREFP I5 (.D(DOUT), .DAC_OUT(DAC_OUT),
               .DAC_OUT_B(DAC_OUT_B), .DB(DB),
               .VREFN(VSS), .VREFP(VREFP));
11 VCO_cell I6 (.ON(ON2), .OP(OP2), .VCTRL(VCTRLN),
               .VSS(VSS), .IN(IN2), .IP(IP2));
12 VCO_cell I7 (.ON(ON), .OP(OP), .VCTRL(VCTRLP),
               .VSS(VSS), .IN(IN), .IP(IP));
13 endmodule
```

One solution to circumvent this problem is to use the multiple supply voltages (MSV) design capability which is available in most APR tools (e.g. Cadence Encounter and Synopsys IC Compiler). The floorplan generation flow is shown in Fig. 10b. The digital gates are assigned to different PDs according to their supply voltag, and the resistors are assigned to different groups according to the resistor types. Note that a PD or a components group may be further partitioned into smaller PDs or components groups to increase the floorplan flexibility.

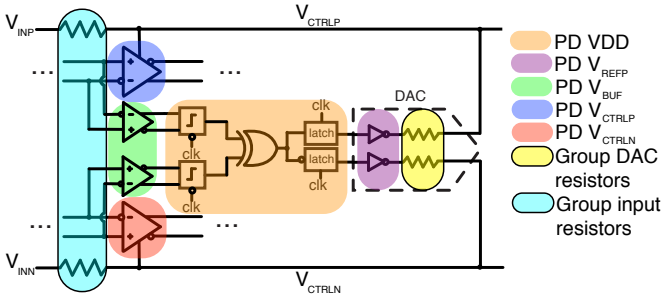
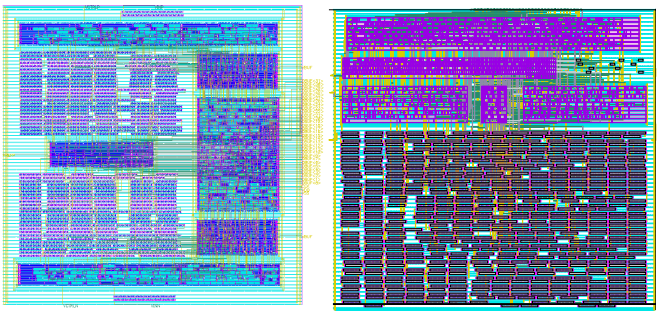


Figure 12: One slice of the ADC decomposed into different power domains and floorplan groups.

4. EXPERIMENTAL RESULTS

Post-layout simulation is performed for both 40-nm and 180-nm CMOS process. The simulation takes into account noise and systematic mismatches, and the architecture is robust against random mismatches as discussed in Section 2.2. The design migration between 40-nm and 180-nm process is done automatically by transforming the standard cells into their closest-size counterparts. The layouts are fully automatically synthesized without manual intervention. The screen captures of the layouts in both process technologies are shown in Fig. 13a and Fig. 13b, respectively. The power domains and components groups could be seen from the resulting layouts. Fig. 14 explicitly indicates them for the 40-nm layout. The circuit is floorplanned such that the placement density is similar in both technology nodes. Since the dimension of the standard cells and other components may scale unproportionally, the circuit floorplan in different process technologies may be different. Thanks to the circuit robustness to layout non-ideality, different floorplans do not influence the circuit performance a lot for the same technology. And that also explains why the proposed circuit is highly suitable for automatic layout synthesis.



(a) (b)

Figure 13: Automatically synthesized layouts in: (a) 40-nm CMOS process. (b) 180-nm CMOS process.

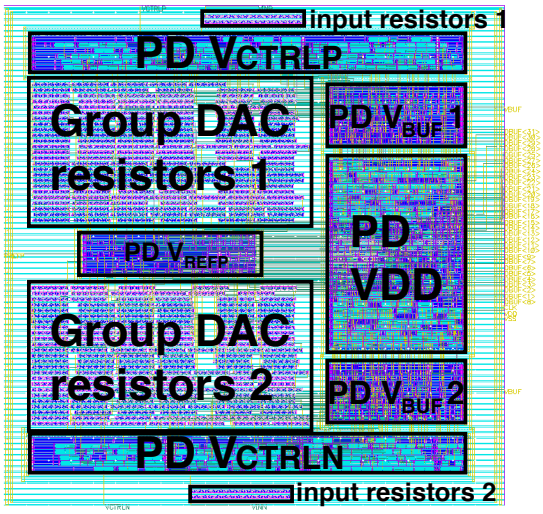


Figure 14: Automatically synthesized layout in 40-nm CMOS process with power domains and components groups indicated.

4.1 Comparisons in Different Process Technology

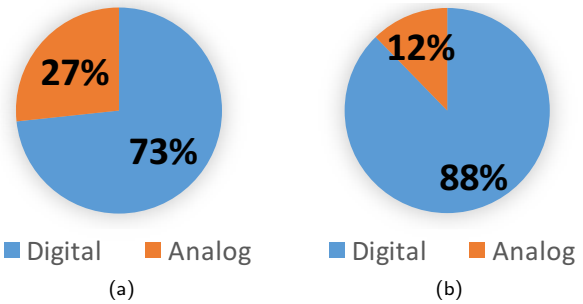
Post-layout transient simulation waveforms of the ADC outputs and the spectra in 40-nm and 180-nm CMOS process are shown in Fig. 16 and Fig. 17, respectively. For the circuit design in 40-nm, $f_{in} = 1$ MHz is set for simulation and that of 180-nm is 250 kHz.

Table 3: Performance comparison between 40-nm and 180-nm process

Process [nm]	fs [MHz]	BW [MHz]	SNDR [dB]	Power [mW]	Area [mm^2]	FOM [fJ/conv]
40	750	5	69.5	1.37	0.012	56.2
180	250	1.4	69.5	5.45	0.151	798

* $ENOB = \frac{SNDR-1.76}{6.02}, FOM = \frac{Power}{2^{ENOB}\cdot 2\cdot BW}$

The circuit performance is desirable. For example, the simulation results for the ADC in 40-nm process show 20dB/dec noise shaping capability. The VCO and DAC mismatches are out of bandwidth (BW), which is 5 MHz for the circuit design in 40-nm process, demonstrating its robustness against non-idealities. The performance of the circuit implemented in 40-nm and 180-nm process are summarized in Table 3. The comparison shows that the proposed circuit not only sees significant power and area reduction, but also a substantial circuit performance improvement expressed by Walden figure-of-merit (FOM [20]) when moving from an older technology node to a more advanced one. Besides, the proposed circuit is also able to work under low input amplitude. Fig. 18 shows the circuit performance of the ADC in 40-nm CMOS process working under input amplitude of 10 mV. No idle tones are observed for the low input amplitude. Further, the power breakdown for both process technologies is calculated (see Fig. 15). It can be seen that the digital portion of the power decreases from 88% to 73%, which is due to the scaling of the digital portion of the circuit. Since the power consumed by the digital portion still occupies 73% of the total power, we can expect to see further power reduction and FOM improvement in more advanced process due to digital scaling. In contrast to the traditional VD-AMS circuits that is incompatible with CMOS scaling, the experimental results demonstrate that the novel TD-ADC enjoys the scaling benefits, and thus is a promising candidate to address the critical real-world challenge of cost-effectively integrating high-performance ADC with digital functions on a system-on-a-chip (SoC).



(a) (b)

Figure 15: Power Breakdown of our ADC circuit in (a) 40-nm CMOS process. (b) 180-nm CMOS process.

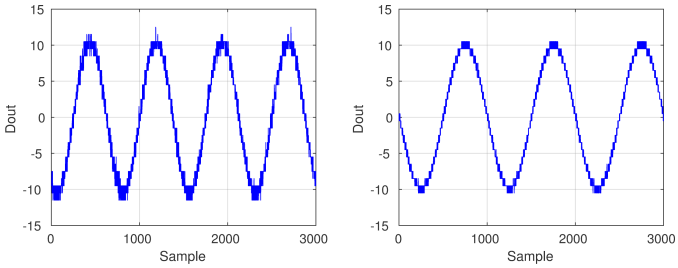


Figure 16: Post-layout transient simulation results of the ADC time-domain outputs in: (a) 40-nm CMOS process. (b) 180-nm CMOS process.

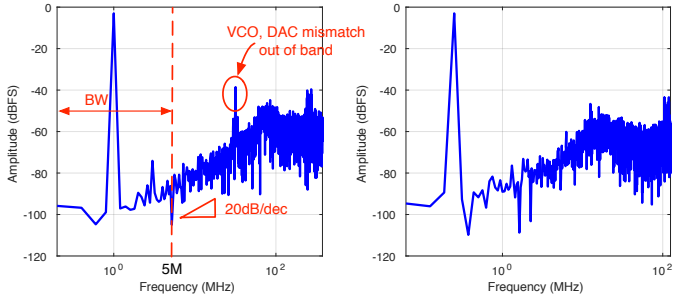


Figure 17: Post-layout simulation results of the ADC spectrum in: (a) 40-nm CMOS process. (b) 180-nm CMOS process.

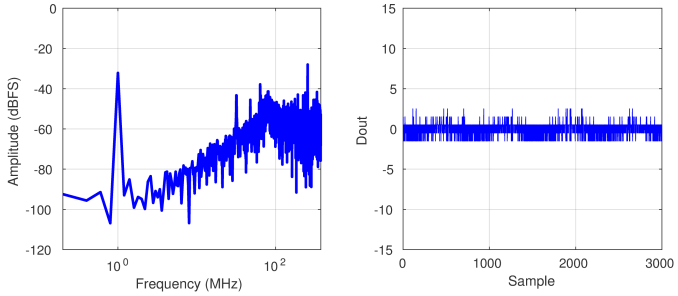


Figure 18: ADC spectrum and time-domain output with low input amplitude in 40-nm CMOS process.

4.2 Comparisons with Previous Works

Table 4 presents the comparisons of our work with previous works of synthesis friendly ADCs. Our work achieves the highest SNDR, which is 13 dB higher than the second best. Being able to achieve a high SNDR of 69.5 dB proves that it is robust against mismatches, and thus, enables the use of digital layout tools for layout synthesis. The overall energy efficiency or FOM of our synthesized ADC is 56.2 fJ/conv-step under post-layout simulation. It compares favorably to the state-of-the-art automatically synthesized ADCs. This demonstrates that the proposed scaling compatible, synthesis friendly ADC design and its synthesis methodology not only significantly improves design productivity and reduces design cost, but also achieves satisfactory circuit performance.

5. CONCLUSION

In this paper, we present a novel scaling compatible, synthesis friendly VCO-based TD $\Delta\Sigma$ ADC, as well as its synthesis methodology. The entire ADC circuit is decomposed into digital gates and a small set of simple customized cells that are added to the standard cell library. Therefore, we are able to leverage the strength of digital APR tools to generate the layout for it. More importantly, the performance of the proposed ADC naturally improves as process technology advances. Experimental results demonstrate its favorable circuit performance, superb scaling compatibility, and an impactful improvement to the synthesis productivity for AMS circuits.

Table 4: Comparisons with previous works

Metric	**This work**	[15]		[16]	[17]
Supply voltage	**1.1**	1	1.2	1.2	1.3
Process [nm]	**40**	65	130	90	180
fs[MHz]	**750**	150	80	210	50
BW [MHz]	**5**	2.34	2	105	25
SNDR [dB]	**69.5**	**56.3**	**56.2**	**35.9**	**34.2**
Power [mW]	**1.37**	0.872	0.983	34.8	0.433
Area [mm^2]	**0.012**	0.014	0.046	0.18	0.094
FOM [fJ/conv]	**56.2**	**348.6**	**466**	**3255**	**204**

* Our reported results are from post-layout simulation. Those from [15–17] are measurement results of fabricated chips.

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