CAD for Double Patterning Lithography

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***Abstract*— *Nanopatterning with 193nm lithography equipment is one of the most fundamental challenges for future scaling beyond 22nm while the next-generation lithography, such as EUV (Extreme Ultra-Violet) lithography still faces tremendous challenges for mass production in the near future. As a practical solution, double patterning lithography (DPL) has become a leading candidate for 16nm lithography process. DPL poses new challenges for overlay control, layout decomposition, and physical design compliance and optimization. In this paper, we will discuss challenges and some recent results in DPL aware timing analysis, layout decomposition, and layout optimization.*

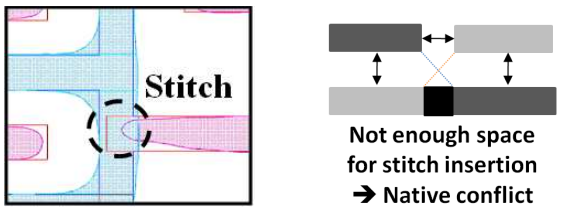
Index Terms— Double Patterning Lithography, Layout Decomposition, Detailed Routing, Layout Optimization

I. Introduction

The mainstream lithography technology using 193nm stepper has been facing severe limitations [1]. One possible solution to overcome the limitation is to use high NA lithography system. Chip makers have been using immersion lithography for sub-40nm patterning which enhances NA from 0.93 (dry) to 1.35 (wet). However, it is hard to find new liquid material to increase NA more than 1.35 in the near future [2]. Electron beam lithography and nanoimprint have their serious limitations due to throughput and mask defects [3] [4]. For the EUV lithography, since the wavelength is 13.5nm, sub-10nm patterning is possible. But EUV lithography still has tremendous technical barriers such as lack of power sources, resists, and defect-free masks [5] [6].

Double patterning lithography (DPL) [7] has been proposed as a strong candidate for 22nm/16nm technology nodes. Double patterning can be implemented in three ways: Litho-Etch-Litho-Etch (LELE), Litho-Freeze-Litho-Etch (LFLE), and Self-Aligned Double Patterning (SADP). LELE uses two lithography exposures and etches on hard-mask to create smaller chip features. LFLE works by freezing the developed resist pattern of the first exposure, then adding a second resist layer immediately on top for the second exposure. The resist pattern is etched at one time after developing. SADP works by depositing a spacer layer over the chip covering all hard mask features. The covered layer is selectively etched away leaving two sidewalls along any ridge, then the ridge is removed [8]. LELE and LFLE require more accurate overlay control to align two exposures [9]–[13]. LFLE uses fewer processing steps [14] [15]. However, LFLE requires insensitive resists between two lithography steps. SADP is only applicable for 1-D patterning having the same transistor length and requires more processing steps such as trimming masks. The overlay requirement of SADP is less stringent than for other double patterning methods. Therefore, SADP is widely used for NAND-flash which has 1-D structures and requires the most advanced technology.

All types of DPL require layout decomposition before manufacturing [16]–[18]. When two features are located closely within the minimum design rule, they need to be decomposed two different masks for LELE and LFLE. SADP also requires layout decomposition to assign a feature to a specific sidewall. During decomposition, coloring conflict can be resolved by inserting stitches. However, minimum stitch insertion is preferred because stitch insertion requires overlap margin, resulting in unwanted chip area increase. In addition, stitches may result in significant printability degradation due to overlay error and line-end effect [19] as shown in Fig. 1(a).



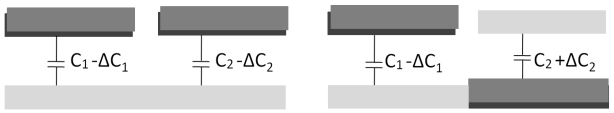
(a) (b)

Fig. 1. (a) Potential yield loss due to stitches, (b) Irresolvable conflict

Several rule-based decomposition methods to achieve minimum stitch insertion have been proposed after placement and routing [20]–[25]. However, decomposition after layout generation may be too late to resolve all the conflicts. Fig. 1(b) shows a case in which stitch insertion cannot resolve a conflict. Such an irresolvable conflict is called a native conflict which can only be removed by layout modification. Therefore, an effort to reduce native conflicts should be taken during placement and routing to shorten design cycle. This paper will discuss the recent achievements on the CAD challenges to enhance decomposability and patterning quality in DPL.

In the rest of this paper, we will survey several analysis issues for DPL in section II. Layout decomposition methods developed recently will be discussed in section III. DPL friendly layout optimization (in particular routing) will be discussed in section IV, followed by conclusion in Section V.

II. Double Patterning Aware Analysis



(a) Decomposition without overlay compensation (b) Decomposition with overlay compensation

Fig. 2. Overlay compensated decomposition.

In [26], Yang et al. propose an overlay aware timing analysis method from measurement of translation, rotation, and magnification overlay, and show that decomposition can play an important roll to compensate the overlay effect in terms of timing variation. Fig. 2 illustrates how to compensate the overlay effect by decomposition. When we do not consider overlay during decomposition, the variation of a coupling capacitance between

two metal layers is in the same direction as shown in Fig. 2(a). Fig. 2(b) shows less timing variation because C_1 decreases when C_2 increases due to overlay error. The paper [26] presents that two adjacent metal layers with overlay consideration may not be parallel any more because overlay effects is different on position by position. Thus, parallel interconnects can be modeled as non-parallel interconnects to consider overlay. In order to use traditional 2.5-D extraction flow, non-parallel conductors need to be converted to parallel interconnects with equivalent spacing to have the same timing behavior. After modeling capacitance with overlay variables, timing analysis for the worst case in terms of overlay can be found by sweeping overlay variables, and determine the variables to make the worst timing behavior. These overlay variables can be used to construct a new equivalent layout with overlay consideration for a timing analysis with overlay.

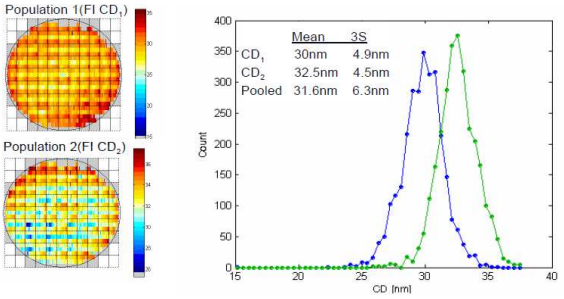


Fig. 3. Bimodal CD distribution shows 8% difference of average.

When gates on a path are correlated spatially, the path delay variation is bigger than the uncorrelated case [27] because the uncorrelated case has more possibility to cancel out. In DPL, the first patterning and the second patterning lose their correlation. Absence of spacial correlation between patterning steps can change the characteristics in terms of timing, power and signal integrity. Fig. 3 shows that mean CD values of two different patterning steps can have 8% difference [28].

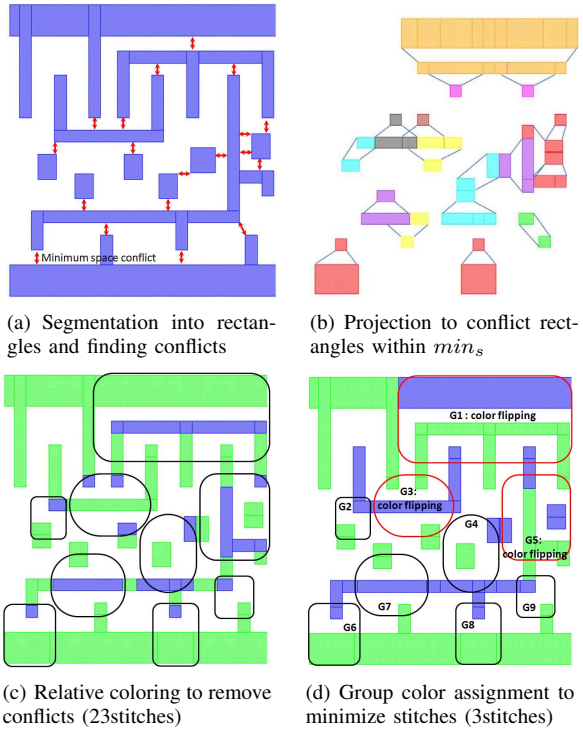
In [29], Jeong et al. assess the timing impact of bimodal CD distribution in DPL, and show that standard cell coloring and placement play a role in reducing the path delay variation. Their experimental results show that different cell coloring in a path can cause 20% path delay variation. Since forcing a feature to have a specific color after placement and decomposition may cause conflicts, Jeong et al. propose layout perturbation to remove the conflicts [30].

III. Layout Decomposition

Layout decomposition is a fundamental step for double patterning lithography which decomposes the original mask into two masks, subject to certain minimum spacing rule constraints. Several papers have been published on rule-based methods [20]–[25]. In [20], Kahng et al. propose a practical double patterning layout decomposition flow. They first apply graph techniques to detect the features associated with irresolvable conflict cycles. When an odd number of conflicts are detected in a conflict graph, a stitch is inserted to break the conflict cycle. Then, the algorithm decomposes a design to minimize the number of stitches based on an integer linear programming (ILP) formulation. Various design constraints, such as minimum width and minimum overlap margin are also taken into account. In [21], Yuan et al. [21] develop an ILP based layout decomposition algorithm for simultaneous conflict and stitch minimization. They also propose several speedup techniques to reduce problem size and improve the runtime and scalability.

Several papers incorporate lithography simulation into their decomposition flow. In [31], Bailey et al. make use of Optical Proximity Correction (OPC) to analyze the quality of the decomposition. The validation result will be returned to the flow for iterative refinement. Chiou et al. [32] further apply a model-based pattern splitting method to locally correct irresolvable coloring errors after rule-based decomposition.

While many previous algorithms mainly focus on stitch minimization with ILP formulations, Yang et al. in [23] propose a fast polynomial time decomposition algorithm with multiple objectives: 1) the number of stitches is minimized, 2) the balance between two decomposed layers is maximized for further enhanced patterning, 3) the impact of overlay on coupling capacitance is reduced for less timing variation. Fig. 4 shows the decomposition steps. A rectangle in Fig. 4(a) is divided into smaller ones based on the projected region from a non-touching neighboring rectangle in Fig. 4(b). The re-segmented rectangles are grouped by traversing non-touching neighbors. In Fig. 4(c), an initial (relative) color is assigned to the rectangles to remove every conflict. There are 23 stitches after relative color assignment which does not consider the stitch minimization. The group color assignment to address multiple objectives is mainly based on a graph theoretical approach which is extended from a min-cut graph partitioning algorithm such as FM [33]. Fig. 4(d) shows the final coloring result after stitch minimization. Fig. 5 shows how to address a decomposition problem into a *min-cut partitioning* problem. The pair of group colors represented by A and $\overline{A}$ is a repulsive pair which should be in different partitions to avoid coloring conflicts. Edge weight between two vertexes means the number of touching pairs between two groups. Fig. 5(a) shows min-cut partitioning and the corresponding decomposed layout for minimum stitch insertion. Fig. 5(b) shows the balanced



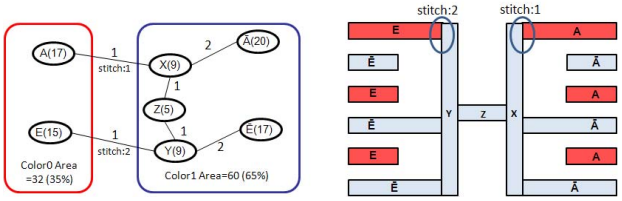
(a) Segmentation into rectangles and finding conflicts

(b) Projection to conflict rectangles within min_s

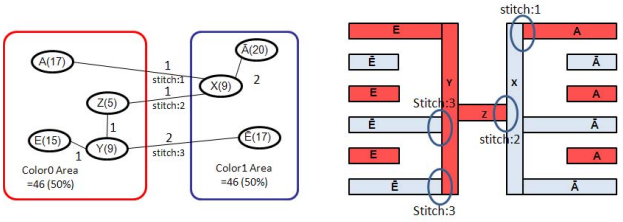
(c) Relative coloring to remove conflicts (23stitches)

(d) Group color assignment to minimize stitches (3stitches)

Fig. 4. Multi-objective decomposition steps of the work in [23]



(a) Min-cut partitioning and the layout



(b) Balanced min-cut partitioning and the layout

Fig. 5. Group color assignment with different partitioning scheme and decomposition results.

partitioning and the decomposed layout which has four stitches.

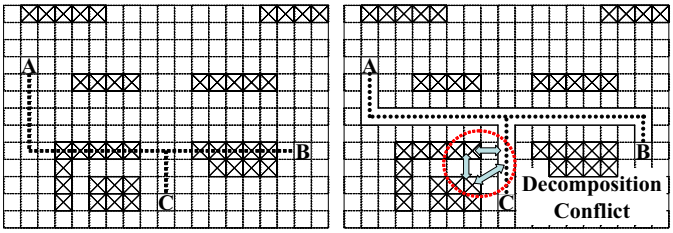
Hsu at al. [34] propose an ILP-based simultaneous layout migration and decomposition for standard cell design. The spacing of polygons are dynamically adjusted for better coloring solution. An effective graph-based reduction technique is also proposed to prune the ILP solution space. In addition, they present an approach to generate DPL-aware standard cells by considering the DPL effects on cell boundaries.

IV. DPL Friendly Layout Optimization

Layout decomposition is a critical step for DPL, especially for highly complex lower metal layers due to 2D patterns. However, layout decomposition itself may be too late if the input layout is not DPL friendly, thus needs co-optimizations from up-stream physical design, in particular, detailed routing. A conventional approach is to first finish detailed routing, then perform layout decomposition. If there is any undecomposable polygon, rip-up&rerouting should be performed to fix the conflict, resulting in long turn-around-time. A detailed routing oblivious DPL may generate highly complex patterns which may increase the indecomposable wire length. In addition, a decomposable layout is not the only objective for successful DPL processes; the number of stitches should be minimized to make a layout robust against overlay error, and so on. Therefore, it is critical to consider DPL optimization in a correct-by-construction manner during detailed routing to achieve multi-objective optimization and faster turn-around-time.

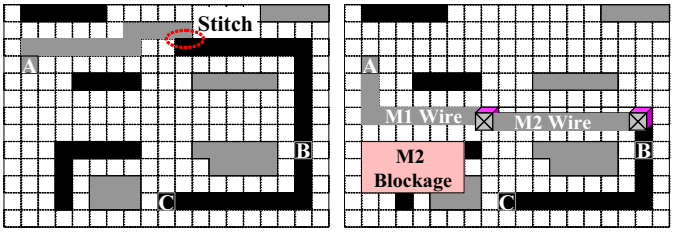
Fig. 6 in [19] motivates why DPL-friendly detailed routing can offer various tradeoffs. For a net A-B-C, its Steiner tree is shown in Fig. 6(a). If a conventional router connects this net, it may generate a solution in Fig. 6(b) which is not decomposable (even with stitches) due to the conflict inside the circle, although it achieves the shortest possible wire length. If DPL-friendly detailed routing is applied to this net, we can get either (c) or (d) which are both decomposable for DPL with different overheads. We have one stitch in Fig. 6(c) but two vias in Fig. 6(d), in order to make a layout decomposable. Therefore, a detailed routing can play a proactive role in improving layout decomposability by exploring the best trade-off among wire length, stitch, and via.

Cho et al. [19] present the first DPL friendly detailed routing algorithm which performs routing and layout decomposition in



(a) Net A-B-C and its Steiner tree with WL=21 in the dotted line are shown. The checked boxes are the blockages on M1.

(b) A routing solution from a conventional detailed router has WL=24, but with decomposition conflicts inside the dotted circle.

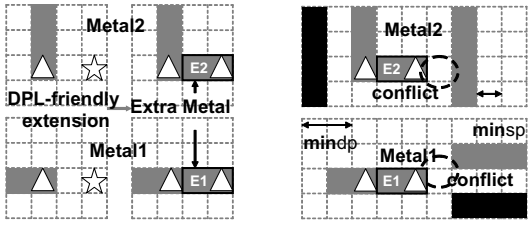


(c) One DPL-friendly solution is shown with one stitch and WL=34.

(d) Another DPL-friendly solution is shown without any stitch and WL=28, but with 2 vias.

Fig. 6. This example motivates DPL consideration during detailed routing.

one shot. The key idea is to perform detailed routing and layout decomposition *simultaneously* in a correct-by-construction manner, in order to accomplish high layout decomposability and reduce the number of overlay-error-prune stitches. While routing a net, the algorithm in [19] finds a path which introduces fewer DPL-related conflicts with the already routed wires. Since decomposition is done along with detailed routing, [19] directly outputs a decomposed layout without an extra time-consuming decomposition step. Experimental results in [19] show that the proposed approach improves the quality of layout significantly in terms of decomposability and the number of stitches with 3.6x speedup, compared with an industrial DPL design flow. Most recently, [35] extends [19] by introducing the concept of lazy decomposition (or lazy coloring). In [19], once a net is routed, the entire wire is decomposed immediately for the minimal number of stitches. However, [35] defers decomposition when decomposition flexibility exists (e.g., a portion of wire which can belong to either mask), and decomposes such deferred cases only if decomposition flexibility is lost due to newly routed wires.



(a) (b)

Fig. 7. Illustration of redundant via DPL-compliance problem

Redundant via, widely used yield improvement technique, could introduce complexity in DPL compliance. Fig. 7(a) [36] shows an example, where the top rectangles are metal2 and the bottom rectangles are metal1. As Fig. 7(a) indicates, E1 and E2 are the extra metals, which are used to cover the via and the redundant via in both layers. To avoid introducing additional stitches, these extensions should have the same color because the metal and the via touch in corresponding layer. However, this may

cause conflicts due to the coloring assignment of existing layout. In Fig. 7(b), the *stitch-free extension* will introduce a conflict in both metal1 and metal2.

As a solution of the problem, Yuan et al. [36] propose a detailed routing framework to perform double patterning lithography and redundant via co-optimization. First, they introduce an ILP based post-routing redundant via insertion algorithm to maximize insertion rate, while introducing zero conflict and minimal extra stitches to existing layout. Moreover, to better resolve this problem in design side, the authors also propose a DPL-friendly detailed router with redundant via consideration. Experimental results in [36] show that the proposed approach improves insertion rate by 43% compared to the case without redundant via consideration, and reduces the number of vias and stitches by 9% and 17% respectively.

V. Conclusion and Future Directions

Double patterning is a leading candidate for 22nm/16nm technology node, and possibly even below with triple or quadruple patterning. In this paper, we show several CAD challenges and recent results, including DPL aware analysis, multi-objective layout decomposition, and DPL friendly routing and compaction. They work together to ensure better variability control and manufacturing yield for DPL. Due to the urgency for DPL deployment in 22nm/16nm nodes, many new capabilities have to be developed and made ready in CAD tools for various DPL processes.

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