Manufacturability Aware Routing

Minsik Cho, Joydeep Mitra, and David Z. Pan
ECE Department, UT Austin

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1 Introduction

Nanometer VLSI design is facing increasing challenges from the manufacturing limitations. These manufacturing/process challenges include the printability issues due to deep sub-wavelength lithography, the topography variations due to chemical-mechanical polishing (CMP), the random defects due to missing/extra material, the via void, and so on. Thus, for nanometer designs, design "closure" may not have the manufacturing closure due to the yield loss. It has been shown, however, that the majority of the yield loss is strongly layout-dependent (as shown by previous chapters), thus manufacturability aware layout optimization shall play a key role in the overall yield improvement.

In this chapter, we focus on manufacturability aware routing. Although there are other manufacturability aware efforts in earlier design stages such as logic synthesis and placement [1–3], routing is often believed to be one of the most effective stages to address the manufacturability issues due to the following reasons [4–7]: (1) the key manufacturing issues (e.g., topography variation due to CMP, random defects, lithography, and redundant vias) are tightly coupled with interconnection network which is mainly determined by routing; (2) routing is the last major VLSI physical design step before manufacturing, thus it has more comprehensive and accurate picture on the expected manufacturability; (3) routing still has considerable design flexibility to find reasonable tradeoff between manufacturability and conventional design objectives (e.g., timing, noise, power). These factors lead to a lot of recent academic and industrial efforts in *manufacturability aware routing*.

In general, routing consists of two steps, *global routing* and *detailed routing*. Global routing plans an approximate path for each net, while detailed routing finalizes the exact DRC-compatible pin-to-pin connections [8]. *Track routing*, as an intermediate step between global and detailed routing, can expedite detailed routing by embedding major trunks from each net within a panel (a row/column of global routing cells) in DRC-friendly manner [9]. Manufacturability aware routing can be accomplished at any stage of routing system if proper manufacturing model is available, and the approaches can be roughly classified into two groups: *rule-based* and *model-based*. The rule-based approach imposes additional manufacturability-driven design rules on a router to avoid manufacturability-unfriendly patterns. The model-based approach utilizes some models to estimate the manufacturability effects to guide router. There are pros and cons for both rule-based and model-based approaches in terms of runtime, scalability, implementation, controllability, and tradeoff, etc.

This chapter will survey recent practices and researches on the manufacturability aware routing. Before discussing key techniques, the major manufacturability challenges for advanced technologies will be discussed in Section 2. Then, we compare the pros and cons of the rule-based approach and model-based approach in Section 3. In practice, both approaches are used where model-based approach can be used for optimization and required rules must be satisfied, in particular, at the detailed routing stage. Section 4 will then go into details of various key aspects of manufacturability aware routing optimizations, including CMP-aware routing, random-defect aware routing, lithography-aware routing, and so on. Section 5 discusses how to deal with manufacturing rules at detailed routing. We will use a few examples to show how rules are becoming more complicated (largely due to the lithography) and the key issues to address them. Finally we conclude in Section 6.

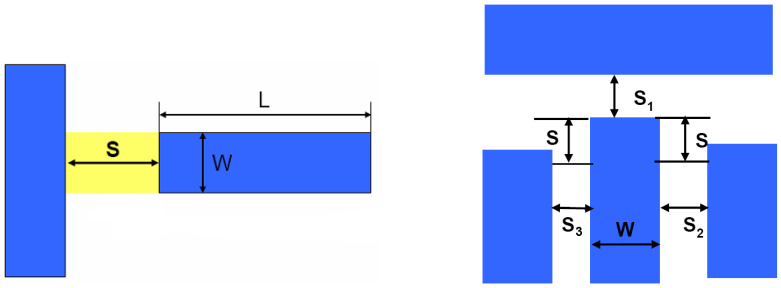
2 Major Manufacturability Issues

In this section, we give an overview of the major manufacturing issues for $90nm$ technology node and below, and analyze the causes and effects of them: (a) printability issues due to sub-wavelength lithography system [10, 11]; (b) random defects due to missing/extra material; (c) topography variations due to chemical-mechanical polishing (CMP), and (d) other causes such as via failure and antenna effect [12, 13].

A fundamental limitation for the *sub-wavelength optical lithography* is WYSINWYG, i.e., "what you see (at design) is not what you get (at fab)". The printability issue arises between neighboring wires/vias due to sub-wavelength effects and process variations. As of now, the $193nm$ (wavelength) optical lithography is still the dominant integrated circuit manufacturing process for $90nm$ and $65nm$ nodes. It is likely to remain so for $45nm$ and $32nm$ technology nodes [14] due to tremendous efforts in the resolution enhancement techniques (RET). However, if the initial design is very litho-unfriendly, even aggressive RET may not be able to solve the printability problem. Thus at the routing stage, it should construct only litho-friendly and printable layouts. It should noted that litho-aware routing is more general than the restrictive design rules (RDR), which has mostly been adopted so far for the poly-layer [15–18].

Smaller feature size makes nanometer VLSI designs more vulnerable to *random defects*, which can be further divided into open or short defect [19, 20]. Both defects are one of the back-end-of-line (BEOL) defects [21], and cause electrical open or short between interconnects. While it is generally believed that the yield loss due to systematic sources is greater than that due to random defects during the technology and process ramp-up stage, the systematic yield loss can be largely eliminated when the process becomes mature and systematic variations are extracted/compensated. On the other hand, the random defects which are inherent due to manufacturing limitations will still be there even for mature fabrication process. Thus, its relative importance will indeed be bigger for mature process with systematic variations designed in [5].

Topography (thickness) variation due to dishing and erosion after CMP is shown to be systematically determined by wire density distribution [22–26]. Even after CMP, intra-chip topography variation can still be on the order of 20-40% [22, 27]. Such topography variation leads to not only significant performance degradation due to increased wire resistance and capacitances, but also acute manufacturing issues like etching and printability due to defocus [22, 25–27]. The main reason for CMP problems is wire density distribution. Higher wire density usually leads to copper



(a) (b)

Description	Rule (µm)
Minimum spacing (S) between a metal and the end-of-line of the metal whose edge width (W) ≤ 0.2 µm	0.14
If a metal of width (W) ≤ 0.2 has neighboring metals along three adjacent edges, then one of the spacings (S_1 or S_2 or S_3) should be ≥ 0.14 µm	0.14
Otherwise, minimum spacing	0.11

Figure 1: Context dependent minimum spacing rule for $65nm$ technology is shown [31]. Each case, (a) and (b) is described in the table.

thickness reduction due to erosion after CMP [23, 24], making resistance worse. Also, the reduced copper thickness after CMP can worsen the scattering effect, further increasing resistance [28].

A via may fail due to various reasons such as random defects, electromigration, cut misalignment, and/or thermal stress induced voiding effects. Redundant via (or double via) can be inserted as a fault-tolerant replacement for the failing one. Redundant via is known to be highly effective, leading to 10-100x lower failure rate [29]. During fabrication process, charges from plasma etching can be accumulated in long floating wires. Such charges may create high current to the thin-oxide gate (Fowler-Nordheim tunneling current), and cause permanent damages to the gate. It is known as the *antenna effect* [13]. There are three kinds of solutions to prevent the antenna effect: protection diode embedding, diode insertion after placement and routing, and jumper insertion. While the first two solutions need extra area for diode, the jumper insertion incurs overhead in routing system due to additional vias [30].

These challenges will be the primary optimization target in manufacturability aware routing, which our discussion in Section 4 and 5 is mainly centered on.

3 Rule-based Approach vs. Model-based Approach

Manufacturability aware routing can be categorized into *rule-based* approach and *model-based* approach. In this section, we discuss the pros and cons of each approach in terms of complexity and efficiency.

Rule-based approach extends the conventional *design rules*, i.e., a set of rules which must be observed by designers/tools, by introducing a new set of manufacturability-aware rules. These new manufacturability aware rules can be *required/hard* rules, or *recommended/soft* rules. Since

existing routing systems have been based on design rules for decades [32], rule-based approach is friendly to the conventional design flow, which makes it seemingly easy to implement and apply. However, there can be several problems with rule-based approach.

1. The number of such manufacturability aware rules is increasing exponentially with each new technology node. For example, while the number of rules is only a few dozen at $180nm$ node, it reaches to several hundred at $65nm$ node and one design rule may work differently depending on the design context.

2. The complexity of checking such rules becomes more computationally expensive, as the rules are increasingly context-sensitive [10, 31, 33]. For example, the minimum spacing between wires may depend on the wire lengths, the neighborhood wires, as shown in an example in Fig. 1. Therefore, simply checking rules by itself needs considerable amount of computing resource.

3. The rules are binary in nature, i.e., either following the rule or violating the rule, thus the rule-based approach does not provide smooth tradeoff.

4. The rules themselves may be too restrictive and pessimistic to sacrifice performance. In some cases, it may be infeasible to achieve the performance goals due to over guard-band from the rules. Furthermore, the rules may not be accurate enough to model very complicated manufacturing processes, in particular for the future deeper sub-wavelength lithography systems.

Due to these limitations of the rule-based approach, there have been significant ongoing efforts in the model-based approach at both academia and industry, expecting that models will capture manufacturing effects more accurately at affordable computational overhead coupled with a small number of simple design rules. For example, this may include lithography system modeling where the light will pass through the mask and react with the chemicals on the surface of the wafer, resulting in printed structures. The challenge with model-based approach is how to abstract a set of reasonably accurate yet high fidelity models at various abstraction levels to guide physical layout optimizations. A typical manufacturing system involves nonlinear optical, chemical, electrical, and mechanical processes which could be extremely complicated to model accurately and mathematically. On the other hand, the models have to be compact and efficient to be embedded in the already time-consuming VLSI routing system. Therefore, the key technical bottleneck for model-based manufacturability aware routing is to develop simple/compact yet effective/high-fidelity models, and apply them to existing routing flow in a seamless manner.

4 Manufacturability Aware Routing Optimization

In this section, we survey key manufacturability aware routing optimization issues on various manufacturability aspects, including topography variations due to CMP in Section 4.1, yield loss due to random defects in Section 4.2, lithography-related printability in Section 4.3, and other issues like via failure and antenna effect in Section 4.4. The optimization may be driven through models or some rules-of-thumb, depending on the nature of the optimization target.

4.1 CMP Aware Routing for Topography Variation Minimization

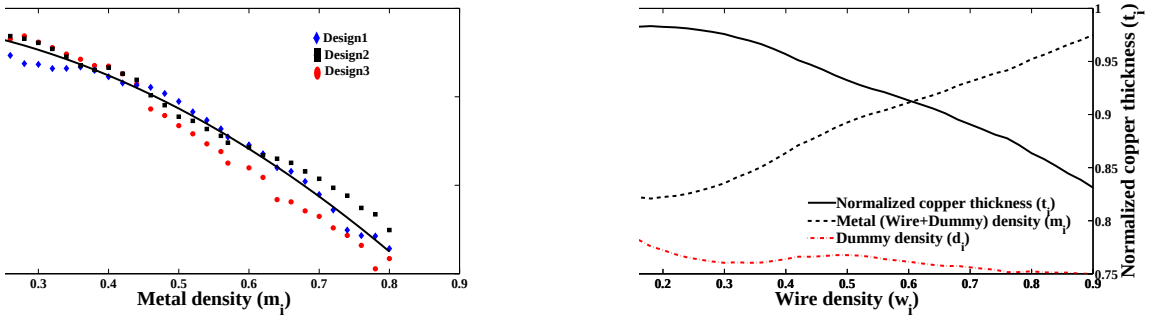
As explained in Section 2, topography variation has significant impact on performance as well as printability. The widely adopted solutions to reduce the topography variation include dummy fill synthesis where dummy features are inserted to increase copper density, and cheesing which creates patterns of holes for fat/wide wires. However, those solutions have inherent limitations, as they are often performed post-tapeout, i.e., on GSDII files to mitigate the problems introduced by the upstream design stages. It shall be more effective if the routing can build in intelligent CMP awareness, in particular at the global routing as CMP-induced variation is a coarse-grained variation.

Regarding design rules on CMP awareness, there is certain maximum density rule requiring that a density within any window of a given size should not exceed the maximum density threshold set by foundry. However, the maximum density rule does not explicitly address topography variation problem, even though it may help to achieve more uniformness by reducing the range of density distribution.

In [6], a predictive copper (Cu) CMP model is proposed to evaluate the topography variation for the first time, and used to guide a CMP aware global routing. Topography variation (thickness variation) after CMP is determined by underlying metal density which includes both wires and dummies. As dummy fill in turn depends on wire density, the required dummy density and the Cu thickness can be predicted from a given wire density. In Fig. 2 (a), normalized Cu thickness change by metal density is shown based on three industrial designs. For a given global routing cell v_i with a metal density m_i, the expected Cu thickness of v_i, t_i can be expressed as follows:

$$t_i = \alpha(1 - \frac{m_i^2}{\beta}) \qquad (0.2 \leq m_i \leq 0.8) \tag{1}$$

where α and β are technology dependent constants. Eq. (1) requires the metal density m_i as an input which is essentially the summation of the wire density w_i and the dummy density d_i in a global routing cell v_i. Fig. 2 (b) shows the required dummy density and the predicted Cu thickness with respect to wire density. For a given v_i, d_i can be looked up with w_i using Fig. 2 (b), and then m_i can be obtained by adding w_i and d_i. Note that metal density in real designs would neither fall below 20% with the aid of dummy fill nor rise above 80% due to cheesing. Finally, the calculated m_i can be fed into Eq. (1) to predict the Cu thickness t_i. This predictive model



(a) Normalized Cu thickness by metal density

(b) Predicted dummy fill density by wire density

Figure 2: Predictive CMP model [6]

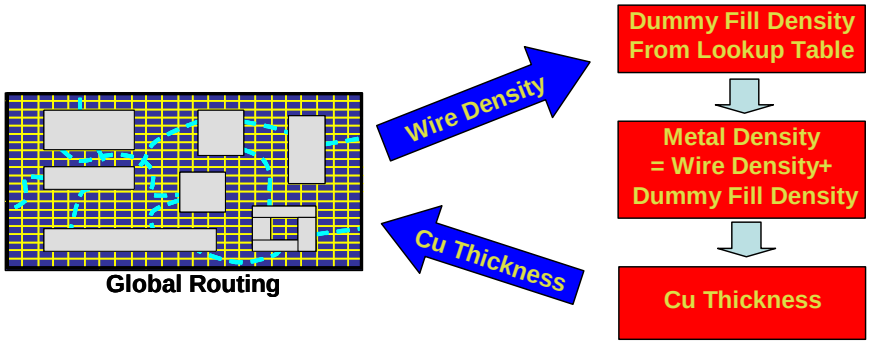


Figure 3: Illustration of CMP aware global routing based on the predictive CMP model [6]

is verified with a commercial CMP simulator [34] and industry test cases. Intuitively, as copper is softer than dielectric material, a region with less copper will experience less erosion during CMP [25]. Therefore, a region with lower metal density will have higher copper thickness, and such region in turn needs more dummies to balance wire density distribution for less topography variation.

The illustration of the CMP aware global routing is shown in Fig. 3 where the predicted Cu thickness guides the global router for less topography variations. A unified metal density driven global router is proposed which not only helps to reduce CMP-induced thickness variation, but also helps to improve timing. Promising experimental results are shown in [6], with 7.510% improvement for topography variation and timing and small runtime overhead.

4.2 Critical Area Aware Routing for Random Defect Minimization

Yield loss due to random defect in general can be minimized by critical area where if a defect of the given size falls, a circuit will be opened or shorted [20, 35]. Due to the criticality of yield in semiconductor industry, there have been considerable amount of efforts to enhance yield by reducing critical area in routing or post-routing. Critical area for a defect is equal to the area where the center of the defect must fall in order to cause a circuit failure for a given defect size distribution. Probability of failure (POF) based on critical area analysis with defect size distribution is a widely used metric for yield prediction and optimization [19, 20]. The defect size distribution $F(x)$ can be modeled as follows [20, 36]:

$$F(x) = kx^{-r} \qquad \text{for } x_{min} \leq x < \infty \tag{2}$$

where x is the defect size, x_{min} is the minimum resolvable lithographic feature size, k is a coefficient to ensure $\int_{x_{min}}^{\infty} F(x)\,dx = 1$, and r ≈ 3 [37]. When the end effect is ignored [38], the critical area $A_i^o(x)$ for open defects on a wire W_i and the critical area $A_{ij}^s(x)$ for short defects between two parallel wires W_i and W_j can be approximated as follows [20, 36, 39]:

$$A_i^o(x) = \begin{cases} 0 & \text{for } 0 \leq x < w_i \\ L_i(x - w_i) & \text{for } w_i \leq x < 2w_i + S_{min} \\ L_i(w_i + S_{min}) & \text{for } 2w_i + S_{min} \leq x < \infty \end{cases}$$

$$A_{ij}^{s}(x) = \begin{cases} 0 & \text{for } 0 \leq x < s_{ij} \\ l_{ij}(x - s_{ij}) & \text{for } s_{ij} \leq x < 2s_{ij} + W_{min} \\ l_{ij}(s_{ij} + W_{min}) & \text{for } 2s_{ij} + W_{min} \leq x < \infty \end{cases} \quad (3)$$

where L_i, w_i, l_{ij}, s_{ij} are the length of wire i, the width of wire i, the overlapped wirelength between wire i and j, and the spacing between wire i and j, respectively. The values of $A_i^o(x)$ and $A_{ij}^s(x)$ will saturate at defect sizes of $2s_{ij} + W_{min}$ and $2w_{iw} + S_{min}$, respectively [36]. The probability of failure due to open defects on W_i (POF_i^o) and due to short defects between W_i and W_j (POF_{ij}^s) on a given layer can be obtained as follows [20, 36]:

$$\begin{aligned} POF_i^o &= \int_{x_{min}}^{\infty} F(x)\frac{A_i^o(x)}{A_{chip}}\,dx = \frac{kL_i}{2A_{chip}}\left(\frac{w_i + S_{min}}{2w_i^2 + S_{min}w_i}\right) \\ POF_{ij}^s &= \int_{x_{min}}^{\infty} F(x)\frac{A_{ij}^s(x)}{A_{chip}}\,dx = \frac{kl_{ij}}{2A_{chip}}\left(\frac{s_{ij} + W_{min}}{2s_{ij}^2 + W_{min}s_{ij}}\right) \end{aligned} \quad (4)$$

where A_{chip} is the total chip area. As POF_i^o and POF_{ij}^s indicate the chance of having a random defect, yield can be improved by minimizing POF_i^o and POF_{ij}^s together, which can be accomplished by maximizing wire width (w_i) and wire spacing (s_{ij}), respectively. However, minimizing POF_i^o and POF_{ij}^s are two conflicting objectives, as larger w_i to decrease POF_i^o leads to smaller s_{ij} which increases POF_{ij}^s with a fixed routing area.

Yield optimization in channel routing is proposed in [40, 41]. Weight interval graph is proposed [40] to facilitate the channel routing algorithm in [42] in a way that net merging in vertical constraint graph will minimize the number of channels as well as critical area. In [41] a wire segment is shifted either from top layer to bottom layer (net burying) or vice versa (net floating) like wrong way routing to reduce critical area in greedy manner. Critical area minimization based on Eq. (4) during global routing is proposed in [43] where a linearized critical area is one of cost factors in multicommodity flow optimization. Redundant link insertion technique to minimize open defect is proposed in [21]. Additional wires will increase the critical area for short defect. Assumption that the probability of failure (POF) due to open defects of a given size is much higher than the POF due to short defects of identical size is not always valid, as it depends on design style as well as process technology [20].

Although some level of critical area reduction is achieved, there are a few drawbacks in these early works which are mostly performed at post-routing or late-stage optimizations: **(a)** one single defect size is considered, rather than a defect size distribution [40, 41], **(b)** the tradeoff between open and short defects due to fixed routing area is ignored [21, 40, 41, 44, 45], **(c)** localized/greedy

$$\begin{aligned} \textbf{min :} \quad & \alpha \textstyle\sum_i POF_i^o + (1-\alpha)\sum_{i,j>i} POF_{ij}^s & \\ \textbf{s.t. :} \quad & |p_i - M_i| \leq d_i & \forall i \\ & S_{min} \leq s_{ij} \leq p_i - p_j - \tfrac{(w_i+w_j)}{2} + (1-o_{ij})N & \forall i,j \\ & S_{min} \leq s_{ij} \leq p_j - p_i - \tfrac{(w_i+w_j)}{2} + o_{ij}N & \forall i,j \\ & o_{ij} \in \{0,1\} & \forall i,j \\ & B_k + \tfrac{w_i}{2} \leq p_i \leq T_k - \tfrac{w_i}{2} & \forall i \in P_k \\ & W_{min} \leq w_i \leq W_{max} & \forall i \end{aligned}$$

Figure 4: Yield-driven track routing formulation in integer non-linear programming [5]

$$
\begin{array}{lll}
\textbf{min :} & \alpha \sum_i \{\delta_i + (1 - \frac{b}{a}) d_i\} + (1 - \alpha) \sum_{i,j} \gamma_{ij} & \\
\textbf{s.t. :} & |p_i - M_i| \leq d_i & \forall i \\
& S_{min} \leq s_{ij} = p_i - p_j - \frac{w_i + w_j}{2} & \forall o_{ij} = 1, \forall j \in n_i \\
& l_{ij} W_{min} \leq s_{ij} \gamma_{ij} & \forall i, \forall j \in n_i \\
& L_i S_{min} \leq w_i \delta_i & \forall i \\
& B_k + \frac{w_i}{2} \leq p_i \leq T_k - \frac{w_i}{2} & \forall i \in P_k \\
& W_{min} \leq w_i \leq W_{max} & \forall i
\end{array}
$$

Figure 5: Yield-driven track routing in SOCP with a given wire order [5]

optimization is performed, which may be suboptimal [21, 44, 46–48], **(d)** wire adjacency information is not available for accurate critical area estimation [38, 43].

In [5], the random defect issue is addressed at the track routing stage which provides reasonable details to model random-defect induced yield loss while it provides much more flexibility than the detailed-routing or post-routing optimization. It proposed a TROY algorithm based on mathematical programming and graph theory to find the best tradeoff between open and short defects w.r.t a defect size distribution through effective *wire planning* (wire ordering, sizing and spacing). Fig. 4 shows the mathematical formulation for the yield-driven track routing. However, this formulation is an integer non-linear programming problem which is prohibitively expensive to solve. However, the key strategy in [5] is that POF_i^o and POF_{ij}^s in Eq. (4) can be simplified into simpler convex forms as in Eq. (5) and if the wire-ordering o_{ij} (thus, n_i as well) is known, the wire sizing and spacing problem for yield optimization can be formulated as the *second order conic programming* (SOCP) as shown in Fig. 5, which can be solved optimally and efficiently. The wire ordering optimization is performed by finding the minimum Hamiltonian path. The experimental results are promising, with 18% improvement in terms of yield loss.

$$
\begin{array}{lll}
POF_i^o \approx & \frac{kL_i}{2A_{chip}} (a \frac{S_{min}}{w_i} - b) & (1 \leq \frac{w_i}{S_{min}} \leq 40) \\
POF_{ij}^s \approx & \frac{kl_{ij}}{2A_{chip}} (a \frac{W_{min}}{s_{ij}} - b) & (1 \leq \frac{s_{ij}}{W_{min}} \leq 40)
\end{array} \tag{5}
$$

4.3 Lithography Aware Routing for Printability

Optical projection systems in modern optical lithography technology usually use partially coherent illumination. An illustration of a typical optical lithography system is shown in Fig. 6. Since a partially coherent system can be approximately decomposed into a small number of P fully coherent systems [4, 49], the aerial image intensity $I(x, y)$ at the point (x, y) can be shown as follows by approximating Hopkins equation [50] through the kernel decomposition [51]:

$$
I(x, y) = \sum_{i=0}^{P-1} | \sum_{j \in W_{(x,y)}} (F_j \odot K_i)(x, y)|^2 \tag{6}
$$

where K_i is the transfer function for the $i-th$ fully coherent optical subsystem, F_j is the transmission function (1 over clear regions and 0 over opaque regions) of the $j-th$ rectangle in effective window $W(x, y)$, the intensity support region of the control point at location (x, y). The size of the

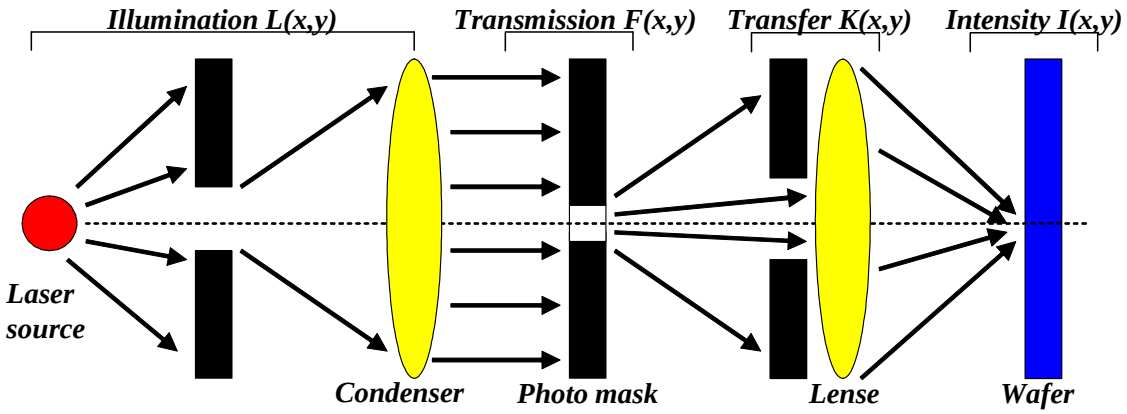


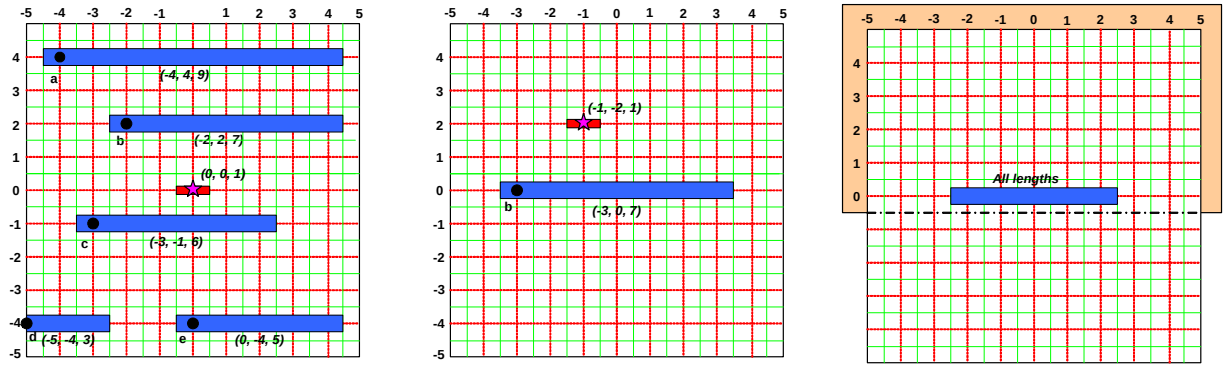
Figure 6: Illustration of optical lithography system for VLSI manufacturing

$W(x, y)$ depends on the wavelength and numerical aperture of the optical system, but in general is about 1-4um. Based on Eq. (6), lithography simulations can be performed to obtain aerial images and then printed silicon images.

The first attempt to address the lithography problem in routing is the OPC aware maze routing work in [4]. Based on aerial image simulation, it stores the expected OPC cost in a lookup table, which has the information on the interference from patterns at different length by distance. While routing a new pattern, the interferences from all existing patterns in its influence window are looked up from the table, then summed up to evaluate the total optical interference from existing patterns. Meanwhile, the optical interference (OPC cost) on existing patterns due to the new pattern is estimated using the maximum interference on these patterns. Fig. 7 shows an example of optical interference lookup table. Then, a vector-weighted graph method is applied to map the grid routing model to a graph, where the edge cost is a vector consisting of the interferences from existing patterns as well as the interference of a new pattern to existing patterns. With such vector-weighted graph, OPC aware maze routing can be casted as multi-constrained shortest path problem which is then solved by Lagrangian relaxation. It shall be noted that optical interference is not a direct lithography metric, such as the edge placement error (EPE) widely used in OPC algorithms.

Another lithography aware maze routing algorithm is proposed in [52] where a table of EAD (electric amplitude of diffraction) is pre-built, and the OPC error is estimated as the square of the accumulated EAD values from the patterns within process window. Then, it greedily performs maze routing such that a routed path for each net does exceed neither OPC error threshold nor path length constraint. Again, it shall be noted that the EAD square metric is not a direct/verified lithography measurement.

The RADAR work [7] is the first attempt to directly link a lithography simulator (using the direct edge placement error metric) to the detailed routing. Based on fast lithography simulation techniques which are more suitable for full-chip simulations, it generates the so-called lithography hotspot maps to guide the post-routing optimization, namely wire spreading and ripup/rerouting. As an example to measure the lithography and RET effort, the edge placement error (EPE) metric is used. To compute EPE efficiently, [7] utilized effective kernel decomposition method and fast table-lookup techniques. In the kernel decomposition based simulation, a core computational step



(a) Five patterns are within the effective window of the edge $(0, 0)$. Each effective pattern is denoted by the left most edge coordinate and its length. For example, pattern a starts at $(-4, 4)$ with length 9.

(b) The optical interference from pattern b on point $(0, 0, 1)$ on can be computed by placing b in the center of the effective window while maintaining the relative location to $(0, 0, 1)$. The interference value can be obtained from the lookup table

(c) The optical interference is simulated for all lengths of patterns centered at the origin, and the interference information on every point above each pattern is kept in the lookup table.

Figure 7: Example of optical interference lookup table [4]

is the convolution term. Due to the linearity of convolution in Eq. (6), the convolution for any arbitrary rectangle inside the effective window can be decomposed into four upper-right rectangles which can reduce the table size significantly [7], as shown in Fig. 8. Therefore, the linear combination of the convolutions of $R1$, $R2$, $R3$, and $R4$ can be used to compute the aerial image of R. After the EPE map is obtained from fast lithography simulations, wire spreading and ripup/rerouting can be applied to reduce the EPE hotspots and to improve printability. The fast lithography simulator is called during the routing modification if needed to make sure no new lithography hotspots occur. Fig. 9 shows an example of RADAR for EPE hotspot reduction. The result implies that both wire spreading and ripup/rerouting are effective in reducing EPE hotspots, but ripup/rerouting can be more effective than wire spreading with less wirelength overhead.

Similar ripup/rerouting approach is proposed later on in [53]. But different from [7], effective pattern searching is adopted, i.e., a set of known undesirable patterns are stored/matched to identity lithography hotspots. Then, the identified undesirable routing patterns are either removed or modified by performing ripup/rerouting. Recently, a multilevel routing approach to minimize the number of OPC features is studied in [54]. A simple OPC cost which becomes higher for longer and wider wires is proposed, and applied as a factor in maze routing. It shall be noted that the lithography aware routing is still in its infancy, and there are many research issues to achieve a holistic understanding for it.

4.4 Redundant-Via and Antenna-Effect Aware Routings

The first redundant-via aware routing is presented in [12]. The problem is formulated as multi-objective maze routing by assigning double-via cost to the routing graph, and solved by applying Lagrangian relaxation technique. In [29], the redundant via is reflected as a factor in the maze routing cost. Each original via has different number of possible redundant via locations, namely

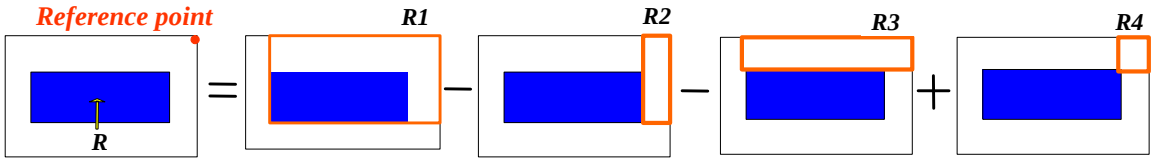
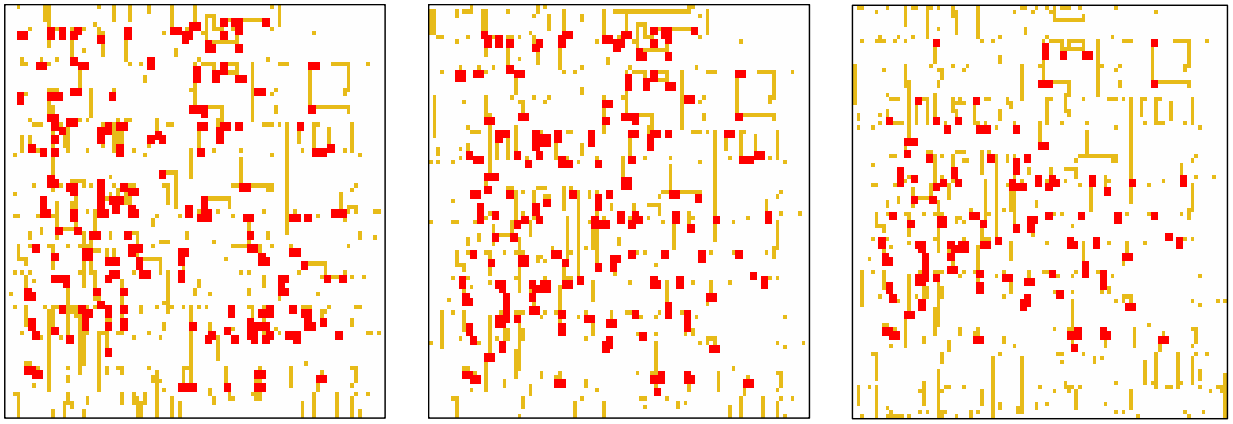


Figure 8: Convolution lookup for fast lithography simulation [7]



(a) EPE hotspots of the initial routing after design closure is shown.

(b) Wire spreading results in 12% EPE reduction with 10% WL increase.

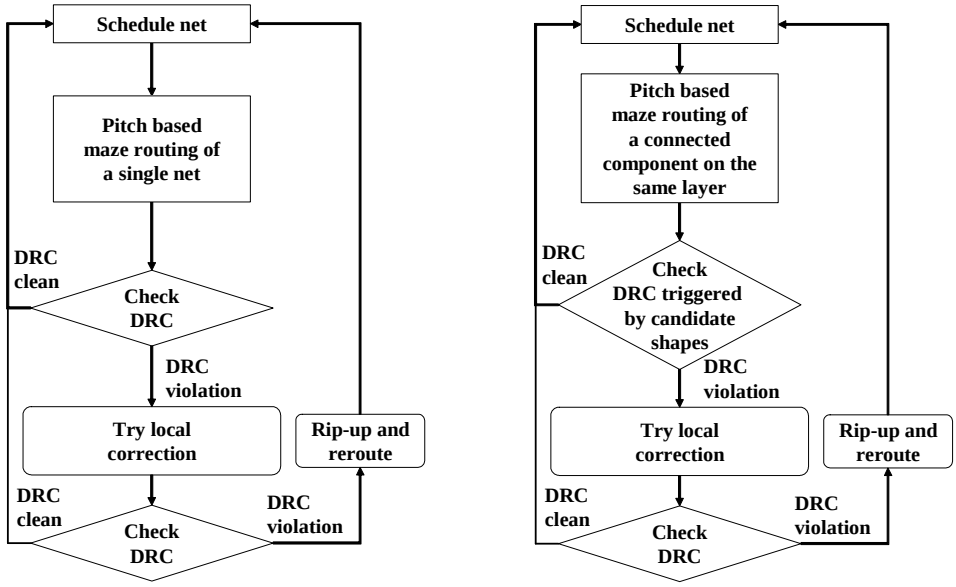
(c) Ripup/rerouting results in 40% EPE reduction 5% WL increase.

Figure 9: RADAR example [7]

degree of freedom (DOF). Wherever the wire occupies a possible redundant via location during maze routing, it is inversely penalized by DOF of its corresponding original via.

In post-layout optimization, redundant-via insertion is one of the key steps for yield improvement. In [55], the redundant via insertion is formulated as a maximum independent set (MIS) problem, and solved by heuristic approach. Different redundant via insertion based on geotopography information is proposed in [56] where a redundant via is tried for each original via in a greedy manner. However, as excessive number of vias can even worsen yield, redundant via insertion under via density constraint is required which is addressed in [57] based on integer linear programming.

While via failure can occur during either fabricating or operating a chip, antenna effect occurs during manufacturing process. The first work in antenna avoidance is presented in [58] and further improved later [59] where ripup/rerouting strategy is used. Another work on antenna avoidance during full chip level routing is discussed in [60]. While these works try to address antenna effect during routing, there are another set of works to fix antenna issue during post-layout optimization as in redundant-via insertion. In [61], antenna avoidance is achieved by a layer assignment technique based on tree partitioning. Regarding diode and jumper insertion, the research in [62] proposes a diode insertion and routing algorithm by using minimum cost network flow optimization, and [63] proposed an optimal algorithm for jumper insertion. However, both the diode and jumper insertion approaches only try to fix antenna problem either by diode or jumper insertion alone. The interaction between diode and jumper insertion is not taken into consideration, as diode



(a) 90nm node and above (b) 65nm node and below

Figure 10: A typical DRC correction flow for a grid-based detailed routing system. The DRC check is more complex in 65nm and below than 90nm and above.

or jumper insertion can be cheaper than one another depending on the design context. The work in [64] combines diode and jumper insertion for optimal simultaneous diode/jumper insertion, based on minimum cost network flow optimization.

5 Dealing with Manufacturing Rules at Detailed Routing

The previous section mostly focuses on manufacturability/yield optimization during routing at various routing stages, driven by certain manufacturing models/metrics or rule-of-thumbs. While their main purpose is to improve manufacturability at the global scope, the final detailed routing still has to satisfy all the required design rules set by manufacturers. These rules are contracts/guarantees from manufacturers. For nanometer designs, these required rules are becoming more and more complicated. On top of the required rules, there can be many even more complicated recommended rules for manufacturability enhancement. This is a topic with very few publications, but it is often a designer's nightmare due to design rule explosions at the detailed routing level.

In this section, we will use several representative design rules (in a progressive more complex manner), extracted from advanced technologies and illustrate how they are becoming more complicated, and how to deal with them at a typical grid-based detailed routing. Actually some complex design rules, when decomposed, each may be equivalent to several simpler rules at early technology generations. The detailed routers could handle them either during the initial route creation process or iteratively through a subsequent ripup/reroute step. But in either case, it is a tedious and time-consuming process.

As design rules become more complex with each technology node, the effort of making detailed router free of these complex design rule violations increases exponentially. Previously what could

be achieved simply by following minimum spacing requirements by keeping routes on certain uniform pitch is no longer sufficient under complex design rules in 65nm and below. It is necessary to monitor design rule compliance much more frequently. As shown in Fig. 10, for 90nm and above, the DRC compliance check is triggered usually *after* the routing for the entire net, but for 65nm and below, such check is needed *during* the routing of the net, e.g., for all the connected components of the net on the same layer, before going to the next layer, and so on. In the worst case, such DRC checking could happen after every routing rectangle is dropped by the router. The main issue and tradeoff are then how to properly select the triggering events for DRC violations. This is mainly based on the candidate shapes being dropped, such as vias which may trigger a minimum edge rule check, as to be explained soon. Also, routers need to select DRC correction schemes which are manufacturing friendly, as several correction alternatives may exist. For example, it may be possible to select vias which introduce the least number of vertices by selecting vias whose landing pads are aligned with the adjacent routing segments.

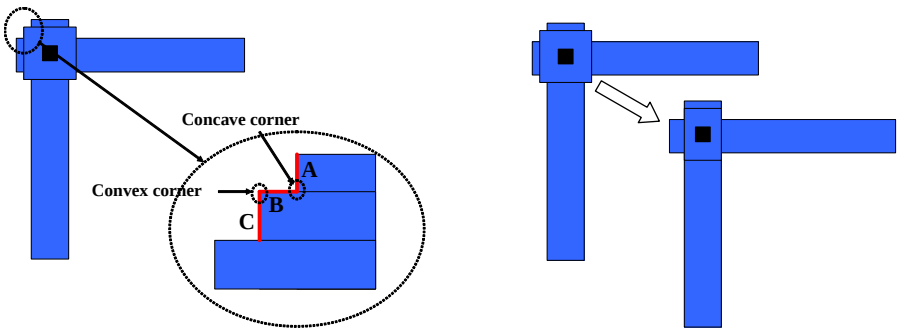
We will now examine three representative classes of complex rules to get a flavor of the level of complexity that the newer generation of routers have to deal with. Each class is progressively more complex than the previous one. The first class of rules is just limited to violations on the same signal net. The second class of rules limits the violations to two signal nets. The third class of rules introduces violations between three or more signal nets.

5.1 Representative Rule 1 - Minimum Edge Rule

An example of the minimum edge rule is shown in Fig. 11 (a) [65]. This rule essentially forbids the formation of consecutive edges with length below certain minimum threshold length *T*. This minimum edge design rule applies to physical components of the same signal net. First, we define the concave and convex corners in Fig. 11 as the corners with both adjacent edges less than the minimum threshold length *T*. There may be several variations of minimum edge rule, depending on the process technologies and routing layers where routing DRC is performed, e.g., any of the following three situations may be a minimum edge rule violation:

- Rule 1a: Formation of any concave or convex corner is a design rule violation.
- Rule 1b: The number of consecutive minimum edges (i.e. edges with length less than T) should be less than certain number (≥ 2). Otherwise, it is a design rule violation. Essentially compared to Rule 1a, Rule 1b may allow formation of concave and/or convex corners up to certain point.
- Rule 1c: The same situation as in Rule 1b, but it further requires that the sum of these consecutive minimum edges is greater than another threshold for design rule violation. For example, in Fig. 11 (a), there are three highlighted edges, A, B, and C which all are minimum edges. If $A + B + C$ is larger than the threshold value, it will cause a design rule violation. Otherwise, it is not.

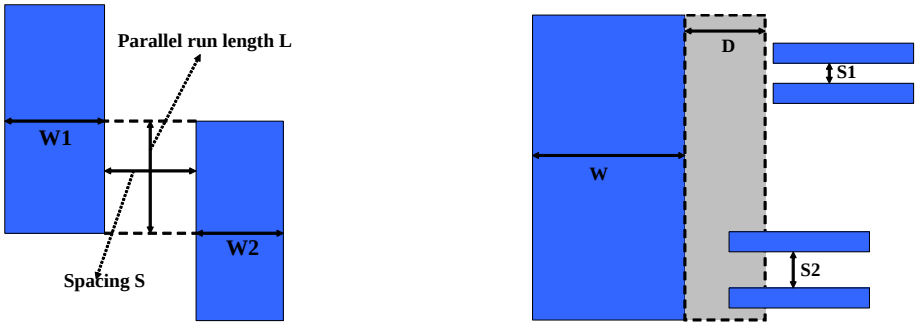
As can be seen from Fig. 11 (a), this rule checking requires a router to perform a polygon analysis of composite shapes, to keep routes free of this design rule violation during routing construction. The challenge for a detailed router is when to trigger this analysis, as this is a rule for the same signal net and is polygon-based whereas the routing shapes are usually rectangles. If



(a) minimum edge rule violation (same net)

(b) shape alignment to fix (a)

Figure 11: An example of the context dependent minimum edge rules for 65nm technology.



(a) width-dependent parallel-length spacing rule

(b) width-dependent influence spacing rule

Figure 12: An example of the context dependent spacing rules for 65nm technology.

the router is symbolic and center-line based, it needs to maintain a history of recent shapes that it has dropped in order to have enough information to perform this analysis. A history of only the previous shape will not suffice, since several overlapping shapes may comprise of a composite polygonal shape which leads to this violation. Therefore, the router needs to maintain a history of at least three previous rectangles that it has dropped, in order to construct a composite polygon and detect the minimum edges. Also, the router need to choose the proper correction method to remove any minimum edge violations that may have been introduced. Several competing solutions may exist, such as shape alignment as shown in Fig. 11 (b), via rotation or even rerouting. The challenge would be how to select the most manufacturing-friendly one. All of the above detection and correction schemes are computationally intensive, and the router needs to have a proper tradeoff between optimization during route creation or post-route correction.

5.2 Representative Rule 2 - Width-Dependent Parallel-Length Spacing Rule

A second class of complex design rules - width dependent parallel-run-length spacing rule, is shown in Fig. 12 (a) [65]. This is a spacing rule between two neighboring physical shapes on dif-

ferent signal nets. The spacing requirement changes depending on the context of the two physical shapes. If the width of either of the two shapes ($W1$ or $W2$) are within a certain range and the parallel run length (L) is also within a certain range, then the spacing (S) between the two shapes has to be greater than a certain threshold. There may be different spacing thresholds for various combinations of the ranges of the widths and lengths between the two shapes. In other words, this class of rules may be decomposed into two or more rules such as:

- Rule 2a: If $A_1 \leq (W_1, W_2) \leq B_1$ and $C_1 \leq L \leq D_1$, then $S \geq S_1$.
- Rule 2b: If $A_2 \leq (W_1, W_2) \leq B_2$ and $C_2 \leq L \leq D_2$, then $S \geq S_2$.

The challenge for the router in this case is that this design rule involves both polygonal analysis within the connected physical components of the same signal net as well as area queries between different signal nets in order to detect violating neighbors. Again, as in the minimal edge rule situation, a composite polygon and in particular wide wire of interest may be formed as the router may drop several overlapping shapes which trigger this rule checking/fixing. Hence, the router first needs to detect the formation of a composite wide wire and once detected, an area query needs to be triggered to detect neighbors within the specified spacing threshold. Triggering a query based on composite wide wires while they are formed may not be sufficient, because new neighbors may be dropped later on (it is shall be noted that one of the two objects needs to meet the width threshold, not both). Therefore, to be safe, the router may need to either perform more frequent checks or perform a check at the end of completion of a fully connected physical component on the same layer. In this case, the only possible post-route corrections are reducing wire widths or rerouting. Hence, once again, several tradeoffs between correct-by-construction routing and post-routing optimization or a hybrid approach need to be considered.

5.3 Representative Rule 3 - Width Dependent Influence Spacing Rule

The third complex design rule involves with three or more nets, described as a width dependent influence spacing rule shown in Fig. 12 (b). It is more complicated than Rule 1 which involves only a single composite shape, and Rule 2 which involves the interaction between two disjoint objects/nets. Rule 3 involves the interaction of two or more shapes in the presence of a third composite wide shape. This rule has the following complex context:

- A wide wire whose width (W) is greater than some threshold.
- Two or more shapes within a halo distance (D) of the above shape.
- The spacing (S) between these two shapes being less than some threshold.

If *all* of the above three situations occur simultaneously, we have an influence spacing rule violation. Again, we first need to detect a wide wire shape, which can be from several composite shapes. Since the rule violation has three conditions, the DRC checking may need to be triggered if any of the above three situations occur which in the worst case could be during the dropping of any shape by the router. But doing such exhaustive checking would be too expensive. A reasonable trigger might be during the formation of a wide wire. However, as in the case of the parallel run-length rule, a neighbor within the halo distance D may appear after the wide wire has been

formed. Thus, this is not a sufficient check. The router may also choose to be conservative and forbid any neighbor wires to enter the halo distance D regions from any wide wires, but this may lead to routability issues since we miss a lot of routing opportunities where this rule is not violated indeed. Therefore, the runtime and performance tradeoff would be a major issue.

So far, we have discussed several representative required design rules in nanometer designs. In addition to hard constraints, nanometer designs (in 65nm and below) have many manufacturability related recommended and soft rules for potential yield improvement, such as multi-cut redundant vias, vias with fatter enclosures, via and metal density requirements, and so on. There are also some soft constraints for preferred versus non-preferred routing directions. For example, routes in the non-preferred direction or jogs are recommended to have wider widths due to poor printability in the non-preferred direction by specific lithographic systems. Manufacturability aware routers shall attempt to follow these recommended rules, but not mandatory since there may be too many to follow, or too hard to implement them efficiently in the already highly-complicated routing system.

6 Conclusion

Design for manufacturability (DFM) in nanometer IC designs has been drawing a lot of attentions from both academia and industry due to its significant impact on manufacturing closure. This chapter surveys various key issues in manufacturability aware routing, a crucial step in the DFM landscape, including model-based manufacturability optimization and rule-based yield improvement, as well as issues of how to deal with complex design rules. While most current DFM solutions rely on either rule-based optimization or post-layout enhancement guided by modeling, there are tremendous ongoing research and development to capture the downstream manufacturing/process effects, and abstract them early on into the key physical design stage, through model-based manufacturability aware routing optimization [4–7, 53]. This will allow designers to perform more global optimization for manufacturability/yield in the context of other design objectives such as timing, power, area, and reliability. For rule versus model, we believe that the rule-based and model-based approaches will co-exist and co-evolve. Ultimately a simple set of rules combined with powerful models would be ideal.

As manufacturability aware routing is still at its early stage under heavy research, there are a lot of rooms to improve in terms of both process modeling/abstraction and DFM-routing algorithms/interfaces, to enable true design for manufacturing [66]. Most current optimizations for DFM are performed independently, but different DFM issues are indeed highly related with each other such as critical area, lithography, CMP, and redundant via. Improving one aspect (e.g., critical area) may make other aspects (e.g., lithography) worse, and vice verse. Therefore, holistic modeling and optimization of all key DFM effects into some "global" yield metric will be in great demand. This should be a future direction for manufacturability aware routing.

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