

INTERCONNECT PERFORMANCE ESTIMATION MODELS FOR SYNTHESIS AND DESIGN PLANNING

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ABSTRACT

The objective of this work is to provide simple, efficient, yet reasonably accurate interconnect performance estimation models for synthesis and design planning under various complex interconnect optimization techniques. We have developed a set of closed-form delay estimation models as functions of interconnect length as well as some other key interconnect and device parameters with the consideration of various interconnect optimization techniques, which include optimal wire-sizing (OWS), simultaneous driver and wire sizing (SDWS), and simultaneous buffer insertion/sizing and wire sizing (BISWS). These models have been tested on a wide range of parameters and shown to have about 90% accuracy on average when compared with the delays obtained by running complex optimization algorithms directly followed by HSPICE simulations. Moreover, our models run in constant time for all practical purposes. As a result, these simple, fast, yet accurate models are expected to be very useful for a wide variety of purposes, including layout-driven logic and high level synthesis, performance-driven floorplanning, and interconnect planning.

1. INTRODUCTION

As VLSI circuit design advances to deep sub-micron (DSM) technologies, interconnect has become the dominating factor in determining the overall circuit performance. As a result, it impacts all aspects of the design flow. In recent years, many interconnect optimization techniques, including interconnect wire sizing, driver sizing, buffer insertion and sizing, etc., have been proposed and shown to be very effective for interconnect delay reductions (see [1, 2] for comprehensive surveys).

However, in the current VLSI design flow, interconnect optimization is usually done at very late stages. Consequently, accurate interconnect performance, especially that for global interconnects is not known to logic/high level syntheses and floorplanning tools. Since interconnect optimization may improve interconnect performance by a factor of 5 to 6 \times [2, 3], it is less likely for synthesis and design planning tools to make correct decision without proper modeling of the impact of interconnect optimization. A brute-force integration that runs existing interconnect optimization algorithms directly at the synthesis and design planning levels may not be practical in designing complex DSM circuits due to the following reasons:

- **Inefficiency:** Most interconnect optimization algorithms use either iterative local refinement operations or dynamic programming based approaches. Although shown to be polynomial in time complexity, they are still too costly to be used repeatedly by logic and high level synthesis engines and/or design planning tools.
- **Lack of abstraction:** To make use of those optimization programs, a lot of detailed information is needed, such as the granularity of wire segmentation, number of wire widths and buffer sizes, etc. However, such information is usually not available during the synthesis and planning level.
- **Difficulty to interact synthesis engines with layout optimization tools.**

To deal with these problems, we develop in this work a set of fast and accurate interconnect delay estimation models under various optimization techniques, namely optimal wire sizing (OWS), simultaneous driver and wire sizing (SDWS), and buffer insertion, sizing and wire sizing (BISWS). Note that most previous layout-driven logic/high level synthesis works, such as [4, 5], often use over-simplified models which assume that the interconnect delay is proportional to the square of wire length, without considering the interconnect optimization. We observe that this quadratic delay model (based on some nominal wire width) can be 5 \times larger than the final optimized delay [2, 3]. Therefore, it is no longer accurate to guide the synthesis tools in deep submicron designs.

Our closed-form delay estimation models overcome all three difficulties listed above: (i) their running time is very low (in constant time in practice), mainly by the complexity of finding the root of some non-linear equations; (ii) they provide abstraction and do not need detailed information such as wire segmentation, number of wire width, etc.; (iii) they can be easily embedded into any synthesis engine. More detailed discussion of applications of our performance estimation models will be given in Section 6.

The rest of the paper is organized as follows. Section 2 states the problem formulation and parameters used for our study. Sections 3 to 5 present the delay estimation models under OWS, SDWS and BISWS respectively, and compare them with HSPICE simulations after running corresponding optimization algorithms using the UCLA Tree-Repeater-Interconnect-Optimization (TRIO) package [2]. Section 6 presents concluding remarks and possible applications of our models.

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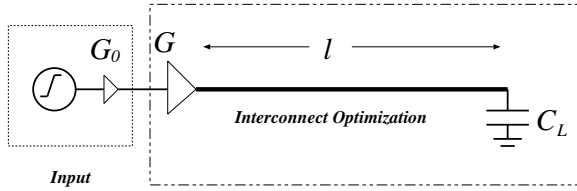


Figure 1. An interconnect wire of length l and loading capacitance of C_L . It is driven by a gate G with input waveform provided by the nominal gate G_0 , which is connected with a ramp voltage input.

2. PROBLEM FORMULATION AND PARAMETERS

The objective of our study is to quickly and accurately estimate interconnect delays with consideration of interconnect optimization. Fig. 1 shows such an interconnect wire of length l to be considered. It is driven by a gate G , and has loading capacitance C_L . G 's input waveform is generated by a nominal gate G_0 connected with a ramp voltage input. The delay to be minimized is the overall delay from the input of G_0 to the load C_L , while the delay to be measured and estimated is the stage delay from the input of G to C_L , denoted as $T(G, l, C_L)$. The input stage delay is included during the optimization so that it acts as a constraint to avoid over-sizing G in the optimization of the stage delay $T(G, l, C_L)$. Our goal is to develop simple closed-form formula and procedure to efficiently estimate $T(G, l, C_L)$ with consideration of various interconnect optimization techniques such as OWS, SDWS and BISWS.

A long wire may be divided into a number of segments during the interconnect optimization. A wire segment is then modeled as a π -type resistor-capacitor (RC) circuit and a buffer is modeled as a switch-level RC circuit (e.g., see [1] for details). Therefore, it will form a distributed RC tree. The well-known Elmore delay model [6] is used to guide the delay optimization and estimation.

The notations of key parameters are listed below.

- W_{min} : the minimum wire width, in μm
- S_{min} : the minimum wire spacing in μm
- r : the sheet resistance, in Ω/\square
- c_a : the unit area capacitance, in $fF/\mu m^2$
- c_f : the unit effective fringing capacitance¹, in $fF/\mu m$
- t_g : the intrinsic device delay in ps
- c_g : input capacitance of a minimum device, in fF
- r_g : output resistance of a minimum device, in $k\Omega$

The values of these parameters for our study are shown in Table 1. They are based on the 1997 National Technology Roadmap for Semiconductors (NTRS'97) [8] and derived in [3]. In the table, the interconnect capacitances are obtained using a 3D capacitance solver FASTCAP [9] for an interconnect wire of $5\times$ minimum width and with two parallel neighboring wires of $5\times$ minimum spacing. The device used for our study is a buffer, made up of two cascaded inverters with stage ratio of 1:5. The device parameters are obtained through HSPICE simulations (with minor adjustments to the data in [3]).

¹It is defined as the sum of the fringing and coupling capacitances, as introduced in [7].

Tech. (μm)	0.25	0.18	0.15	0.13	0.10	0.07
W_{min}	0.25	0.18	0.15	0.13	0.10	0.07
S_{min}	0.34	0.24	0.21	0.17	0.14	0.10
r	0.0733	0.0679	0.0733	0.0806	0.0917	0.0952
c_a	0.0589	0.0596	0.0542	0.0461	0.0531	0.0558
c_f	0.0819	0.0641	0.0538	0.0433	0.0448	0.0404
t_g	86.6	66.4	65.5	54.4	50.1	29.8
c_g	0.282	0.234	0.220	0.135	0.072	0.066
r_g	16.2	17.1	17.3	22.1	23.4	22.1

Table 1. Interconnect and device parameters based on NTRS'97.

3. DELAY ESTIMATION MODEL UNDER OPTIMAL WIRE-SIZING (OWS)

In this section, we present the delay estimation model under OWS. It was first shown in [10, 11] that when wire resistance becomes significant, as in deep sub-micron designs, proper wire-sizing can effectively reduce the interconnect delay. Assuming that each wire has a set of discrete wire widths, their work presented an optimal discrete wire-sizing (DWS) algorithm for a single-source RC interconnect tree to minimize the sum of weighted delays from the source to timing-critical sinks under the Elmore delay model. It was extended to optimize a routing tree with multiple sources [12], and to minimize the maximum delay using Lagrangian relaxation [13]. An alternative approach to perform wire-sizing optimization is through bottom-up dynamic programming [14] and it can be combined easily with routing tree construction and buffer insertion [15]. Later on, optimal continuous wire sizing (CWS) for a wire segment was studied. Closed-form wire shaping functions was obtained to minimize the Elmore delay, first without fringing capacitance [16, 17], later on with fringing capacitance [18, 19], and recently for a bi-directional wire [20].

Our detailed study first shows very close matches between CWS and DWS in terms of the resulting delays after optimization (see [21] for details). Therefore, in the following discussions, we will just use OWS for either CWS or DWS. For OWS, the size of driver G in Fig. 1 is fixed. Let R_d be the effective resistance of G , $T_{ows}(R_d, l, C_L)$ be the delay under OWS for an interconnect l with driver resistance R_d and loading capacitance C_L . We have performed extensive analytical and numerical studies on the original complex wire shape and delay functions under CWS [18, 20] and extracted the key terms that contribute to the optimal OWS delay as follows.

$$T_{ows}(R_d, l, C_L) = (\alpha_1 l / W^2(\alpha_2 l) + 2\alpha_1 l / W(\alpha_2 l) + R_d c_f + \sqrt{R_d r c_a c_f l}) \cdot l \quad (1)$$

where $\alpha_1 = \frac{1}{4} r c_a$, $\alpha_2 = \frac{1}{2} \sqrt{\frac{r c_a}{R_d C_L}}$, and $W(x)$ is Lambert's W function [18] defined as the value of w that satisfies $w e^w = x$.

The justification for Eqn. (1) can be found in [21]. When the fringing capacitance is zero, it consists of the first two terms and degenerates into the closed-form optimal Elmore delay formula under CWS without fringing capacitance, as shown below:

$$T_{ows}(R_d, l, C_L)|_{c_f=0} = \alpha_1 l^2 / W^2(\alpha_2 l) + 2\alpha_1 l^2 / W(\alpha_2 l) \quad (2)$$

The last two terms in Eqn. (1) are the adjustment terms

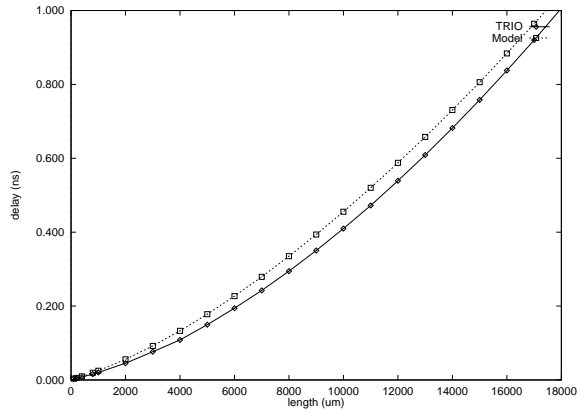


Figure 2. Comparison of the delay estimation model with running TRIO under OWS using the 0.18 μm technology. $R_d = r_g/100$, $C_L = c_g \times 100$.

when considering the fringing capacitance. From the definition of the convex function and the characteristics of the W function, we can easily show that

Proposition 1 T_{ows} is a sub-quadratic convex function with respect to the interconnect length l . \square

This characteristic of T_{ows} will be useful to perform optimal buffer insertion and wire sizing (BIWS) in Section 5.

We have tested the closed-form delay estimation model in Eqn. (1) on a wide range of parameters. It matches the optimal delay very well from running TRIO package under OWS optimization, with about 90% accuracy on average. An example with typical interconnect parameters is shown in Fig. 2. In these experiments, we have wire width set being $\{W_{min}, 2W_{min}, \dots, 20W_{min}\}$ and the wire is segmented into $10\mu\text{m}$ -long segments.

4. DELAY ESTIMATION MODEL UNDER SIMULTANEOUS DRIVER AND WIRE SIZING (SDWS)

This section presents the delay estimation model under SDWS, which sizes both the wires and the driver. The SDWS problem was first studied in [22]. It was shown that the dominance property presented in [11] still holds for SDWS problem and the local refinement operations (as used by OWS) can be used iteratively to compute tight lower and upper bounds of the optimal widths for the driver and wires efficiently. However, it has not been possible to develop a closed-form solution from the local refinement based iterative algorithm.

To obtain an accurate delay estimation model, we use the OWS delay estimation model from the previous section. Note that in our problem formulation, G_0 is fixed. But the driver G can be sized optimally to achieve the best performance from available driver set D . Denote R_{d0} and R_d to be the effective resistance of G_0 and G , and C_d to be the input capacitance of G . Suppose G 's size is $k \times$ minimum device. From the switch-level device model, we have $R_d = r_g/k$ and $C_d = kc_g$. Then the overall delay from the input of G_0 to C_L in Fig. 1 to be minimized is

$$\begin{aligned} T(k) &= (t_g + R_{d0} \cdot C_d) + t_g + T_{ows}(R_d, l, C_L) \\ &= (t_g + R_{d0} \cdot kc_g) + t_g + T_{ows}(r_g/k, l, C_L) \end{aligned} \quad (3)$$

Delay Estimation Model under SDWS	
Input:	$R_{d0}, l, C_L, c_a, c_f, r, \text{ and driver set } D \text{ of size between } [k_{min}, k_{max}]$
1.	Calculate the best driver size k_{opt} that minimize $T(k)$ of Eqn. (3) <ul style="list-style-type: none"> - calculate the root k^* of $dT(k)/dk = 0$ - if $k_{min} < k^* < k_{max}$, k_{opt} is one of $\lfloor k^* \rfloor$ or $\lceil k^* \rceil$ which gives smaller $T(k)$ - else k_{opt} is one of k_{min} or k_{max} which gives smaller $T(k)$
2.	Compute T_{sdws} using Eqn. (4)

Figure 3. The Delay Estimation Model under Simultaneous Driver and Wire Sizing.

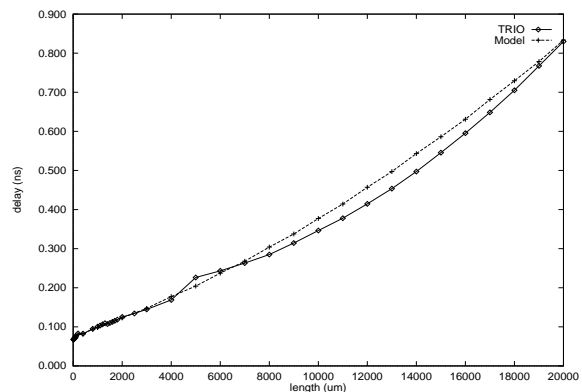


Figure 4. Comparison of the estimation model with running TRIO under SDWS using the 0.18 μm technology. G_0 and C_L are based on a $10 \times$ minimum device.

under the constraint of given driver choices. Note that the input stage delay ($t_g + R_{d0} \cdot C_d$) is included for overall delay minimization. Substitute the delay formula of T_{ows} from (1) and calculate the best driver size k_{opt} that minimizes $T(k)$, we can obtain the delay estimation under optimal SDWS,

$$T_{sdws}(D, l, C_L) = t_g + T_{ows}(r_g/k_{opt}, l, C_L) \quad (4)$$

Recall that we do not include the input stage delay in our delay estimation. The simple delay estimation procedure under SDWS is outlined in Fig. 3. To solve the root k^* of $dT(k)/dk = 0$, we can use the efficient numerical approach such as bisection method [23]. Let ϵ_0 be the initial range that k^* lies in and ϵ be the error tolerance for k^* . Bisection method basically cuts the root search range by half at each iteration. So the number of iterations will be $\log_2(\epsilon_0/\epsilon)$. In practice, ten or less iterations are usually sufficient for the root-finding. Therefore, for all practical purposes, the procedure in Fig. 3 can be considered to run in constant time.

Fig. 4 compares the optimal delay from our estimation model and that from running TRIO package under SDWS using the 0.18 μm technology. Our delay estimation model matches the experimental results very well, with over 90% accuracy on the average.

5. DELAY ESTIMATION MODEL UNDER BUFFER INSERTION/SIZING AND WIRE SIZING (BISWS)

BISWS is a more powerful technique that can further reduce interconnect delay than SDWS by allowing buffer insertion to divide long wires into shorter ones. A polynomial-time dynamic programming based algorithm was first presented in [24] to find the optimal buffer placement and sizing for RC trees under the Elmore delay model. It was further extended to include simultaneous buffer insertion and wire-sizing [14]. In this section, we will first introduce the concept of critical length for buffer insertion under OWS and give an analytical formula for it. Then we derive a delay estimation model for buffer insertion and wire sizing (BIWS, no buffer sizing), and for buffer insertion, sizing and wire sizing (BISWS).

5.1. Critical Length for Buffer Insertion under Optimal Wire Sizing

Given the delay estimation model $T_{ows}(R_d, l, C_L)$ in Eqn. (1), we can analyze the longest wire that can run without the benefit from buffer insertion. For a buffer b with intrinsic delay of T_b , input capacitance of C_b and output resistance of R_b , denote $T_{1buf}(\alpha, R_d, l, C_L)$ to be the delay by inserting one such buffer at the position of αl from the source ($0 \leq \alpha \leq 1$). Then

$$T_{1buf}(\alpha, R_d, l, C_L) = T_{ows}(R_d, \alpha l, C_b) + T_b + T_{ows}(R_b, (1 - \alpha)l, C_L) \quad (5)$$

is the delay after inserting one buffer into the wire with OWS of the resulting two wire segments. We can find the α that minimizes the $T_{1buf}(\alpha, R_d, l, C_L)$ by solving the root of $dT_{1buf}/d\alpha = 0$ under $0 \leq \alpha \leq 1$, denoted as α_{opt} . Then it is beneficial to insert such a buffer into a wire of length l , loading capacitance of C_L and driver resistance of R_d if and only if the resulting delay is smaller than the optimal wire sizing delay, i.e.,

$$T_{1buf}(\alpha_{opt}, R_d, l, C_L) < T_{ows}(R_d, l, C_L) \quad (6)$$

We define the *critical length* for inserting buffer b to be the minimum l that satisfies Eqn. (6) and denote it as $l_{crit}(b, R_d, C_L)$.

Intuitively, when the wire length l is small, optimal wire sizing will achieve the best delay; whereas when the interconnect is long enough, the buffer insertion becomes beneficial. Thus, the root of l for the following equation

$$f(l) = T_{1buf}(\alpha_{opt}, R_d, l, C_L) - T_{ows}(R_d, l, C_L) = 0 \quad (7)$$

gives the critical length for buffer insertion, i.e., $l_{crit}(b, R_d, C_L)$. The critical length computation procedure is outlined in Fig. 5. Similar to SDWS, we use very fast bisection method [23] to obtain the root for Eqn. (7). Let ϵ_0 be the initial root range and ϵ be the error tolerance for l_{crit} , the root can be computed in $\log_2(\epsilon_0/\epsilon)$ iterations in step 2. In practice, a conservative estimation of $\epsilon_0 = 2cm$ and a error tolerance of $\epsilon = 10\mu m$ are usually sufficient enough for our delay estimation purpose, which leads to about 11 iterations for computing $l_{crit}(b, R_d, C_L)$. Therefore in practice, the procedure in Fig. 5 can be considered to run in constant time.

We notice that in a very recent work by [25], critical length concept was also introduced but based on a different assumption. In [25], buffer insertion was performed on a *uniform* wire line, whereas ours is performed together with

Procedure to Compute $l_{crit}(b, R_d, C_L)$	
Input:	R_d, C_L , and buffer b with characteristics of R_b, C_b and T_b
/* Use bisection (binary search) method */	
1.	initialize l_{crit} 's range $[l_{min}, l_{max}]$, where $f(l_{min}) > 0$ and $f(l_{max}) < 0$
2.	while $l_{max} - l_{min} > \epsilon$ $l_{mid} \leftarrow (l_{min} + l_{max})/2$ if $f(l_{mid}) > 0$, $l_{min} \leftarrow l_{mid}$ else $l_{max} \leftarrow l_{mid}$
3.	return l_{mid}

Figure 5. The procedure to compute critical length for buffer insertion.

Tech. (μm)	0.25	0.18	0.15	0.13	0.10	0.07	
[25]	2.52	2.23	2.14	1.94	1.50	1.43	
Ours	10 \times	4.12	3.80	3.97	3.61	2.92	2.08
	50 \times	6.40	5.81	6.01	5.51	4.45	3.30
	100 \times	7.47	6.83	7.04	6.39	5.30	3.91
	200 \times	8.65	7.92	8.14	7.43	6.35	4.49
	500 \times	9.98	9.10	9.30	8.57	7.13	5.21

Table 2. Critical length l_{crit} (in mm) for buffer insertion under uniform min wire width based on [25] and under OWS based on Eqn. (7) with some typical buffer sizes from 10 \times to 500 \times min device.

OWS. In [25], an important observation is that l_{crit} is independent of buffer size. However, this is not the case for our l_{crit} where OWS is performed. As a comparison, Table 2 shows the critical lengths for various NTRS'97 technology generations using the formula of [25] under uniform minimum wire width (MIN) and using our procedure in Fig. 5 under some typical buffer sizes. It is interesting to observe from that: (i) l_{crit} decreases as technology further advances. But l_{crit} 's decrease is not as fast as the technology's scaling down. (ii) As l_{crit} decreases and chip size increases [8], more buffers shall be used for performance optimization as the technology scales. So for DSM circuit designs, a long interconnect is no longer a simple metal line but indeed a complex circuitry and needed to be planned carefully! (iii) In contrast to [25], our l_{crit} under OWS is no longer independent of buffer size. Indeed, it tends to increase as buffer size gets larger. (iv) Our l_{crit} under OWS may be significantly larger than that based on MIN. For example in the 0.25 μm technology, l_{crit} under OWS with 500 \times minimum device is 9.98 mm , about 4 times of that based on MIN, which is 2.52 mm .

5.2. Delay Estimation Model under Buffer Insertion and Wire Sizing (BIWS)

In this subsection, we derive the delay estimation model under optimal buffer insertion and wire sizing. We assume that all buffers (including the driver) are of the same size and the size is given *a priori*. We will first provide some theoretical analysis, then give the delay modeling for BIWS.

Proposition 2 For optimal BIWS solution to an interconnect wire, the distance between adjacent buffers is equal.

Proof: We just need to prove that for any internal buffer b (i.e., neither the first or the last), it should be inserted in the middle position of its two neighboring buffers. Since all buffers are of the same size, we just need to minimize

the sum of two OWS solutions before and after the inserted buffer. According to Proposition 1, T_{ows} is a convex function of l . Then, from the definition of the convex function (i.e., $\lambda f(x) + (1 - \lambda)f(y) \geq f(\lambda x + (1 - \lambda)y)$, $\lambda \in [0, 1]$), we have

$$\begin{aligned} & \frac{1}{2}T_{ows}(R_b, \alpha l, C_b) + \frac{1}{2}T_{ows}(R_b, (1 - \alpha)l, C_b) \\ & \geq T_{ows}\left(R_b, \frac{1}{2}\alpha l + \frac{1}{2}(1 - \alpha)l, C_b\right) \\ & = T_{ows}\left(R_b, \frac{l}{2}, C_b\right) \end{aligned} \quad (8)$$

So the best location for the buffer b will be $\alpha_{opt} = 1/2$. That is to say, the buffers will be equally spaced. \square

Remark 1: In [26] and [25], buffer insertion was performed at equal spacing for an interconnect with uniform wire width. It was stated that the number of buffers as well as the delay are linear functions of the interconnect length. The justification of such a conclusion was recently presented in [27]. However, none of [26], [27] and [25] performed optimal wire sizing while doing buffer insertion. From our proof above, it is clear that as long as the wire segment delay is a convex function of l , which is the case for both uniform wire width and optimal wire sizing, we should insert buffers at equal spacing. \square

Given Proposition 2, it is easy to show that

Proposition 3 *The optimal distance between adjacent buffers under optimal BIWS is $l_{crit}(b, R_b, C_b)$.* \square

We simply denote $l_{crit}(b, R_b, C_b)$ as l_c . Then the total number of buffers (including the driver) will be $n_b = \lceil l/l_c \rceil$. They divide the original wire into n_b stages. Each stage has equal wire length of l_c and equal delay of $T_{crit} = t_g + T_{ows}(R_b, l_c, C_b)$ (defined as the *critical delay*), except the last one. Let the length of the last stage wire segment be l_{last} , then $l_{last} = l - (n_b - 1)l_c$, and the last stage delay is $T_{last} = t_g + T_{ows}(R_b, l_{last}, C_L)$. Therefore, the following accurate delay estimation model for BIWS is obtained:

$$\begin{aligned} T'_{biws} &= T_{crit} \cdot (n_b - 1) + T_{last} \\ &= \tau_{biws} \cdot (n_b - 1)l_c + T_{last} \end{aligned} \quad (9)$$

where τ_{biws} is given by the delay estimation model under OWS:

$$\begin{aligned} \tau_{biws} &= t_g/l_c + \alpha_1 l_c/W^2(\alpha_2 l_c) + 2\alpha_1 l_c/W(\alpha_2 l_c) \\ &+ R_b c_f + \sqrt{R_b r c_a c_f l_c} \end{aligned} \quad (10)$$

The model in (9) can be further approximated by the following linear model with respect to l , which usually will be accurate enough for delay estimation purpose.

$$T_{biws} = \tau_{biws} \cdot l + t_g \quad (11)$$

The delay estimation model under BIWS is summarized in Fig. 6. In practice, $l_c = l_{crit}(b, R_b, C_b)$ can be computed in constant time. Eqns. (9), (10) and (11) can also be computed easily in constant time, so our estimation model under BIWS again takes only constant time. For buffer size of $100\times$ minimum, we list l_c and τ_{biws} in Table 3. It shows that the estimated buffer numbers match those given by running BIWS algorithm [2] in TRIO very well, differing by at most one for a global 2cm interconnect. In terms of delay, the model in either (9) or (11) gives very good matches compared with running TRIO as shown in Fig. 7, having about 90% accuracy.

Delay Estimation Model under BIWS	
Input:	$R_{d0}, l, C_L, c_a, c_f, r,$ and buffer b
1.	Compute $l_c = l_{crit}(b, R_b, C_b)$
2.	Compute τ_{biws} using Eqn. (10)
3.	Compute T'_{biws} using Eqn. (9) or T_{biws} using Eqn. (11)

Figure 6. The Delay Estimation Model under Optimal Buffer Insertion and Wire Sizing.

Tech. (μm)	0.25	0.18	0.15	0.13	0.10	0.07
l_c	7.5	6.8	7.0	6.4	5.3	3.9
τ_{biws}	0.53	0.44	0.41	0.39	0.38	0.39
$\lceil l/l_c \rceil$	3	3	3	4	4	6
#BT	4	4	4	4	4	7

Table 3. Results from delay estimation model and running TRIO under BIWS. Buffer size is $100\times$ min. l_c is in mm, and τ_{biws} is in $10^{-4} ns/\mu m$. $\lceil l/l_c \rceil$ and #BT are numbers of buffers inserted for a 2 cm interconnect estimated from the model and obtained by running TRIO, respectively.

5.3. Delay Estimation Model under Buffer Insertion, Sizing and Wire Sizing (BISWS)

The BISWS technique is the most complete and powerful optimization to reduce delay for global interconnects. The optimal delay will be largely dependent of the given buffer choices, which makes the delay estimation modeling more difficult. However, as seen in BIWS, buffer insertion divides the original long wires into smaller segments according to some critical length l_c and shields the quadratic behavior. Therefore we expect that a similar linear relationship between delay and length will still hold for BISWS. This hypothesis is confirmed by Fig. 8, which shows the optimized delay by running TRIO package under BISWS optimization for various technologies in NTRS'97. For all technologies, the buffer size is up to $1000\times$ minimum feature size, and the wire width is up to $20\times$ minimum width.

Then the only unknown to be determined is the slope of the linear function. For a long wire with many buffers, we observe from our running of TRIO package that the internal buffers will be approximately of the same size and of equal distance between adjacent buffers due to their symmetric structure. Therefore, the slope can be estimated using the best BIWS solution from available buffer selections. The delay estimation model for BISWS is thus proposed as follows:

$$T_{bisws} = \tau_{bisws} \cdot l + t_g \quad (12)$$

where $\tau_{bisws} = \min_{b \in B} \{\tau_{biws}\}$ from available buffer set B . The critical length l_c for BISWS is then estimated by the critical length of BIWS with minimum τ_{biws} . The delay estimation model under BISWS is summarized in Fig. 9. It is easy to show that the time complexity of the model is $O(|B|)$, where B is the set of available buffer sizes (usually no more than 20, so the BISWS estimation model can also be considered to run in constant time for practical purpose). The results from the delay estimation model and from running BISWS algorithm in the TRIO package are shown in Table 4 and Fig. 10. The estimation model again closely matches the experimental results.

Remark 2: In [28], the closed-form optimal BISWS solution without consideration of fringing capacitance was de-

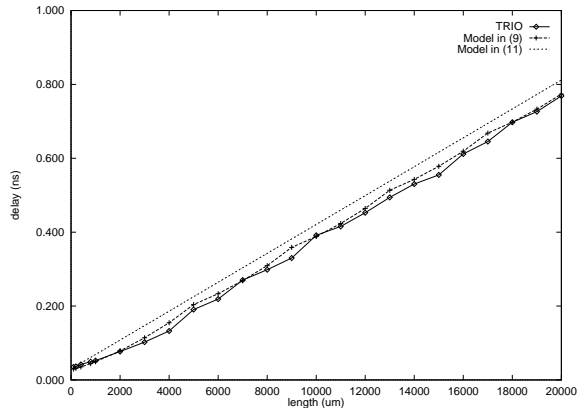


Figure 7. Comparison of delay estimation model with running TRIO under BIWS optimization for the 0.07 μm technology. G_0 and C_L are based on a 10 \times minimum device.

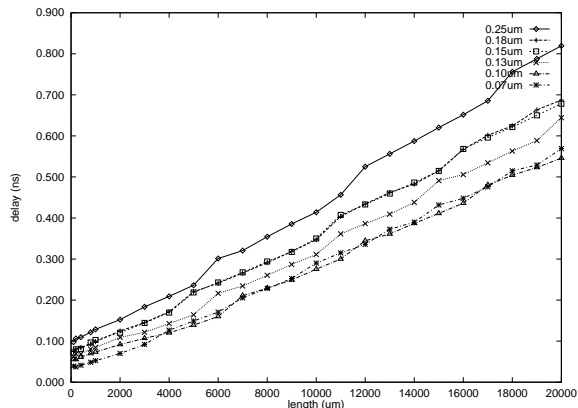


Figure 8. The delay vs. length relationship by using BISWS of TRIO package for various NTRS'97 technology generations from 0.25 μm to 0.07 μm . For all technologies, G_0 and C_L in Fig. 1 are based on a 10 \times minimum.

rived. From their delay formula, we have done analysis and shown the linear relationship between delay and length, which confirms our results. Yet [28] is a special case of our BISWS as we consider both area and fringing capacitances. It is still an open problem to provide a theoretical justification of the linear relation in Eqn. (12) under BISWS in the general case. We are currently studying this problem. \square

6. CONCLUSIONS AND APPLICATIONS

The main contribution of our work is a set of closed-form delay estimation models and very efficient computation procedures (constant time in practice) under various interconnect optimization techniques, such as OWS, SDWS, and BISWS for both local wires (without buffer insertion) and global wires (with buffer insertion). These models match the experimental results very well (with about 90% accuracy on average) and run extremely fast compared with running complex interconnect optimization algorithms (e.g., TRIO) directly. In addition, they can be easily embedded and coded into any synthesis engine and design planning tool.

Delay Estimation Model under BISWS

Input: R_{d0} , l , C_L , c_a , c_f , r , and the buffer set B

1. Compute the $\tau_{bisws} = \min_{b \in B} \{\tau_{bws}\}$
2. Compute T_{bisws} using Eqn. (12)

Figure 9. The Delay Estimation Model under Optimal Buffer Insertion, Sizing and Wire Sizing.

Tech. (μm)	0.25	0.18	0.15	0.13	0.10	0.07
l_c	9.9	9.1	9.3	8.6	7.1	5.2
τ_{bisws}	0.41	0.33	0.33	0.32	0.27	0.28
$\lceil l/l_c \rceil$	3	3	3	3	3	4
#BT	3	3	3	4	3	5

Table 4. Results from delay estimation model and running TRIO under BISWS. For all technologies, G_0 and C_L are based on the 10 \times minimum buffer. The units are the same as in Table 3.

We believe that these delay estimation models can be used in a wide spectrum of applications listed, but not limited, as follows:

- Placement-driven synthesis and mapping: One may keep a companion placement during synthesis and technology mapping [29, 30]. For every logic synthesis operation, the companion placement will be updated. Once the cell positions are known, one can use our delay estimation models to accurately predict interconnect performance and feed it into the synthesis engine.
- RTL and physical level floorplan: During the sizing and placement of functional blocks, one can use our models to accurately predict the impact on the performance of global interconnects.
- Interconnect process technology optimization: Interconnect parameters (e.g., metal aspect ratio, minimum spacing, etc.) may be tuned to optimize the delays predicted by our models for global, average and local interconnects under certain wire-length distributions.
- Interconnect Planning: (i) Various interconnect optimization alternatives can be evaluated for front-end engines to make decision during RTL synthesis and floorplanning. (ii) Based on the back-end interconnect optimization requirements from our estimation models, routing resource as well as silicon real estate (e.g. for buffer insertion) can be planned beforehand.

We plan to extend our interconnect performance estimation models to handle nets with multiple-pin topology in the future. Also, we plan to look at the performance estimation models under area/power constraints.

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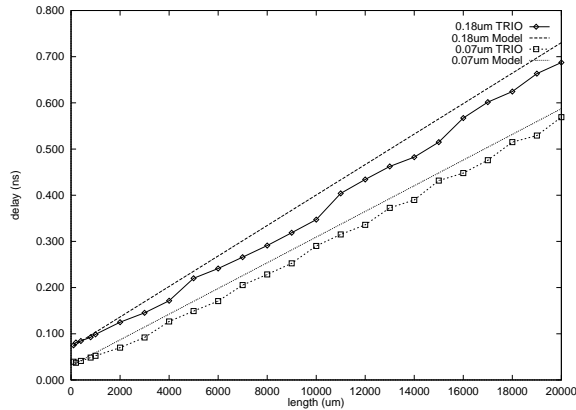


Figure 10. Comparison of delay estimation model and experimental results using BISWS optimization for 0.18 and 0.07 μm technologies.

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