Luigi Capodieci (AMD): *Managed Variability: Present and Future of Design-Process Integration from 45nm, and 32nm, to 22nm and beyond*

Abstract:

The rate of increase of intrinsic variability in semiconductor IC's at 32 and 22nm technology nodes poses a formidable challenge and a few interesting opportunities for high performance designs. While variability has been a constant presence in the semiconductor industry, the approaching end of the "scaling roadmap" makes it necessary to co-develop and co-optimize designs and manufacturing processes, introducing novel CAD methodologies and flows. Current state-of-the art tools allow for accurate characterization of both random and (most importantly) residual systematic variability and this study examines the trend towards design techniques where variability is deliberately assigned to and distributed among functional components and sub-blocks ("managed variability") in order to enable a continued "performance roadmap" even in the presence of a slow-down of the geometric shrink-path. The study concludes by examining potential research directions for the architectural DFM insertion in the design flow.

Samar K. Saha (SilTerra): *Variability in scaled CMOS technology and modeling approaches for circuit simulation*

Abstract:

In this talk, an overview of variability in advanced CMOS devices, impact of variability on device and circuit performance, and the modeling approaches of variability for circuit analysis will be discussed. With the continued scaling of MOSFET devices towards their ultimate dimensions near 10-nm regime, the variability in device performance has become a critical issue in the design of integrated circuits (IC) using advanced CMOS technologies. The increasing complexities in CMOS technology such as strain-silicon channel, halo-doping, ultra-thin gate oxide, ultra-shallow source-drain junction, mili-second annealing, and so on are introducing an increasing number of variability that can no longer be modeled by the conventional worst case design technique. Presently, the increasing amount of within-die variability has imposed an enormous challenge in the conventional design methodology. Due to the variability constraints, a circuit optimized using the conventional design methodology is more susceptible to random fluctuation in delay and therefore, the statistical design methodology has become indispensable for modern IC design. In this presentation, the experimental and theoretical results of variability in advanced CMOS devices and their impact on circuit performance are first described. Then, an overview of different modeling approaches to account for the variability in IC design will be discussed.

Colin McAndrew (Freescale): *Backward Propagation of Variance: You Measure it, BPV can Model it!*

Abstract:

The backward propagation of variance (BPV) technique for statistical modeling arose from a very simple, yet painful, situation: continuously explaining to designers why distributions in parameters like Leff and Tox matched manufacturing perfectly, yet variations in performances like Idsat (key for digital designers) and gm (key for analog designers) did not. Furthermore, why were the modeled variations in these performance different between digital and analog models, whereas of course the manufacturing data to be modeled were the same. The solution to this painful situation was, in hindsight, obvious: compact models are only approximations, so rather than feed in "physical" variations for parameter variations to a model, and get out indeterminate variations in key device electrical performances like Idsat and gm, which will be different for different models, why not feed in real variations in these key performances and then work backwards to calculate the appropriate variations in parameters, which may be different for different models, that are necessary to match the observed variations in the key performances? This concept, BPV, has proved to be highly effective for both global and local (mismatch) statistical variation modeling.

Modern technologies introduce three new requirements to statistical modeling: the need to account for nonlinearities in the mappings from parameters to key device electrical performances; the need to account for the fact that the component of the overall statistical variation due to local variation is no longer small

compared to the global component; and the need to account for correlations between key device electrical performances. It will be shown that all of these new requirements can be incorporated into the basic BPV formalism, and that composite circuit level performances, such as gate delay, can also be included to quantify correlation between NMOS and PMOS devices.

John Krick (TI): *Statistical Transistor SPICE Modeling in Advanced CMOS Technologies*

Abstract:

A key to maintaining high integrated circuit yields is to ensure that the circuits are robust to process variations inherent in the silicon manufacturing process. One of the most powerful tools available to communicate process variations to circuit designers is in the form of a statistical SPICE model. This presentation will provide a high-level overview of the CMOS statistical SPICE modeling approach that has evolved within Texas Instruments over the past six technology nodes with an emphasis on the challenges faced in supporting mixed signal applications in highly integrated system on chip (SoC) designs.

Chenming Hu (UCB): *Compact Models of Some MOSFET Variations*

Abstract:

A compact model for flicker noise in small MOSFETs is developed from some general principles. A non-rectangular gate is developed to link the MOSFET gate shapes produced by fast TCAD simulators with a compact model. The corner-model methodology can be improved by imbuing it with a more quantitative connection to circuit performance. These examples illustrate the diverse opportunities for compact models to contribute to design-for manufacturing.

Josef Watts (IBM): *A Multilevel Approach to Statistical Compact Modeling*

Abstract:

The performance of a given circuit design can be thought of as a multidimensional space where each dimension is a particular metric of performance. Performance metrics can include such things as propagation delay, standby power, noise margin, etc. Likewise device performance can be thought of as a multidimensional space where each dimension is a device characteristic such as threshold voltage, oxide capacitance and mobility. Given a compact model representing a particular point in device (performance) space and circuit netlist a circuit simulator will map that point in device space into circuit (performance) space. Since even identically designed devices on a single die can have different characteristics, the device space of a circuit has a separate dimension for each characteristic of each device.

This allows the circuit designer to verify that the design will meet all of it application requirements i.e. that the mapping is to a point within the allowed region of circuit space. Since a real manufacturing process over time can produce circuits from anywhere within a fairly large volume of device space the circuit designer needs to ensure that every (or nearly every) point the expected design space maps to a point within the allowed region of the circuit space.

This is the purpose of the statistical compact model. How sophisticated a model is required for this task is determined by the complexity of the manufacturing process, the complexity of the circuit space and amount of simulation the circuit design can afford to spend. For static CMOS logic gates where delay is overwhelmingly dominate performance metric it may be sufficient to identify points in the device space which represent three sigma fast and slow delay and ensure that they map to acceptable places in the circuit space. For fine tuning a static RAM cell which will be replicated millions of times on one chip and used in many chip designs a more sophisticated approach which considers differences between instances of identically designed devices will be required.

In this paper we present a methodology for producing a statistical compact model which supports statistical analyses of varying degrees of sophistication. The method begins with the most sophisticated model, a Monte Carlo model incorporating correlations between devices types and devices instances. Various simpler models are generated by applying simplifying assumptions to the most general model.

Xi-Wei Lin (Synopsys): *Modeling of Proximity Effects in Nanometer MOSFET*

Abstract:

As the CMOS feature size scales downward, the electrical properties of a device, such as L, W, mobility, and Vth, become increasingly dependent on its layout context. Three primary sources of the layout proximity effects will be discussed: a) sub-wavelength photolithography, b) strain silicon engineering, and b) ion scattering and transient-enhanced diffusion due to ion implantation. An incremental modeling approach is commonly used to handle the proximity effects. It scales or corrects the model parameters of an existing core compact model for well-defined reference structures. Based on the partitioning of layout extraction and model computation, two methodologies, namely LPE and MBE, can be distinguished for the implementation of the proximity compact models. LPE is conventional and relies on simplification of problems to minimize the performance and capacity impacts to layout extractors and circuit simulators. It runs into limitations as the proximity problems become complex. On the other hand, MBE offloads the computational burdens from LVS netlistor and SPICE simulators, opening the door for more physical, yet simpler, modeling of proximity effects. The EDA flow for addressing the above variability issues will be presented. And examples of WPE and stress effects will be given to illustrate the MBE concept.

Bruce McGaughy (ProPlus): *Model Extraction and Simulation Challenges for Process Variations in 45nm and Below*

Abstract:

The increased impact of process variations in the nanometer is placing greater demands on both the model extraction and circuit simulation domains. The model extraction flows are required to support extraction of growing numbers and types of corner models, as well as support statistical models at the process and mismatch levels. Reliability models add an extra dimension of difficulty. Simulation tools are also expected to provide statistical simulation of process variation and mismatch, as well as deal with reliability with good accuracy and high performance. In addition, there is increasing demand for simulators to support statistical sensitivity analysis, principle component analysis, and deterministic variation of netlist and model parameters.

Kishore Singhal (Synopsys): *Display and Analysis of Variability Simulation Results*

Abstract:

Variability simulations are computationally expensive and generate large volumes of data. Most designers are reluctant to use these techniques because they see little value in them and companies find it hard to justify their investment in statistical modeling. Designers are reluctant to use variability methods because they often lack the necessary background in computational statistics.

In this presentation, I will use examples to demonstrate simple yet effective techniques to display the results of statistical analyses, to relate the precision of the results to the number of samples, the use of statistical sensitivity to identify key devices and parameters that are responsible for response variability, the construction of empirical statistical models, and their use for design improvement.