IEEE/ACM Workshop on Compact Variability Modeling (CVM)
Summary Report

1. Background

It is widely recognized that process variation is emerging as a fundamental challenge to IC design with scaled CMOS technology; and it will have profound impact on nearly all aspects of circuit performance. Although traditionally the negative effects of variation are mostly dealt with during data preparation and/or manufacturing process, the industry is starting to accept the fact that some of the effects can be better mitigated during the design phase. To facilitate robust design for variability, compact variability models are essential to provide coherent and consistent abstraction of the variability so that designers can take them into consideration. As a premium conference on CAD, ICCAD attracts many experts from industry and academia. The purpose of this workshop is to provide a forum for device modeling and CAD researchers and practioners to discuss the current practice and future needs.

2. Workshop Statistics

The Compact Variability Workshop was successfully held at Doubletree Hotel in San Jose on November 13th, 2008. Because this is the very first time, the workshop organizers decided to invite nine speakers from universities and leading semiconductor companies. There were 40 attendees participated the workshop. Four sections were presented on the overall picture of process variations, modeling of variation mechanisms, statistical compact model, and simulation techniques. The detailed agenda was posted at http://www.eas.asu.edu/~ycao/cvm.

3. Technical Summary

The speakers presented a comprehensive view on the variation sources, advanced device modeling for variations, statistical extraction methodology, and simulation techniques. In sub-90nm CMOS technology generations, both the number of variation sources and the amount of variations keep increasing as an inevitable result of continual scaling. Primary reasons include the manufacturing limits, such as sub-wavelength lithography, and fundamental physics limits, such as random dopant fluctuations and the flicker noise. These variations further interact with circuit layout and can be effectively mitigated by careful physical design. Compact variability modeling, which bridges the underlying mechanisms with circuit simulation, needs to be able to timely and accurately capture these variations sources.

During the workshop, several presenters discussed advanced modeling solution for emerging variations, including lithography induced line-edge roughness, non-rectangular gate, statistical flicker noise, and proximity effects (e.g., stress effect and well-proximity effect). It is demonstrated that these new effects can be incorporated into standard CMOS models. With the support from TCAD simulations, these models capture the non-linear behaviors with respect to the operation conditions and enable circuit analysis with the awareness on major variations.

In additional to the physical understanding, the development of variability modeling requires statistical modeling techniques to efficiently extract the essential characteristics and map them into device parameters with sufficient accuracy. Traditional corner based approach may still be able to handle current design needs, if the corners are appropriately defined for a specific design application. Yet in future generations, a true statistical solution is necessary, as the number of corners is rapidly increasing. A couple of statistical modeling approaches were presented, such as Backward Propagation of Variance (BVP). These approaches systematically decompose silicon variations into device model parameters. They are suitable to be implemented into CAD tools to automatically build statistical model.

The problem of variation model further propagates to how to interpret, simulate, and display statistical results. The solution requires joint efforts by CAD tool developers and designers. One important aspect is the mindset to statistically deal with the design. While this concept was hindered by expensive computation cost, we could leverage the improvement in hardware and better develop the statistical design flow.

4. Looking Forward

With ever-increasing process variations, the quality of modeling and design tools is greatly challenged. While significant efforts have been spent on variability modeling, these models need to be abstracted into the design hierarchy in order to make the impact on leading products. This bottom-up abstraction needs to be coupled with silicon characterization and circuit design knowledge such that designers will be able to search the optimal solution with adequate confidence.

Following this conclusion, we plan to continue our workshop next year, with possible joint presentation from test structure design for variations.

5. Acknowledgement

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