2009 IEEE/ACM Workshop on Variability Modeling and Characterization (CVM) Workshop

Summary Report

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1. Background

It is widely recognized that process variation is emerging as a fundamental challenge to IC design in scaled CMOS technology; and that it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distribution. It also requires carefully designed test structures and proper statistical data analysis methods to extract meaningful statistical models from noisy silicon measurements. The resulting compact modeling of systematic, spatial, and random variations is essential to abstract the physical level variations into a format the designers (and – importantly- the tools that they use) can utilize. This workshop provides a forum to discuss current practice as well as near future research needs in test structure design, variability characterization and compact variability modeling.

2. Workshop Statistics

The 2009 Compact Variability Modeling and Characterization (CVM) workshop is the continuation of the successful 2008 event. Based on the attendee feedbacks, the organizers of 2008 CVM workshop and Test Structure Design (TSD) workshop decided to merge the two into a single workshop for 2009. This year, the workshop was successfully held at Doubletree Hotel in San Jose on November 5th, 2009. The combined workshop brought together 34 academic and industrial experts in device modeling, compact modeling, test structure design as well as designers and EDA developers. Due to the late start of this year's workshop, the organizers decided to invite 12 speakers from universities, leading semiconductor and EDA companies to present their latest work on the variability modeling. Four sessions were organized, covering topics in atomic scale modeling, process induced variations, extraction techniques as well as test structure design and measurement. The detailed agenda has been posted on the workshop website http://www.eas.asu.edu/~ycao/cvm

3. Technical Summary

In the morning sessions, the speakers provided a comprehensive overview of intrinsic device fluctuations and manufacturing induced variations. They presented various aspects of device variability and their atomistic level simulations, ideas to mitigate the variability from novel device structures as well as measurements and potential impact of random telegraph noise. The speakers also presented circuit level techniques to reduce circuit sensitivities to variability, methods to extract spatial variation from full wafer perspective, and issues associated with various layout-dependent variations.

In the afternoon sessions, the speakers presented temporal reliability challenges, and massive amount of efforts to characterize them in the industrial setting, as well as the efficient EDA tools

to extract parasitic variations. They also presented novel techniques to minimize the number of manufacturing monitors need to extract variability, and the variability challenges facing standard library based design. The last two presentations in the workshop cover the variability characterization techniques for SRAM devices, as well as aging effects such as NBTI, PBTI and TDDB.

During the discussions in the sessions, it is well recognized among the participants that both static and dynamic variability are getting worse as technology scaling progresses. A particular challenge ahead is how to effectively manage the variability issues in the design stage. At the device level, fundamental models of certain phenomena, such as random telegraph noise, are vitally needed. There is also the challenge on how to integrate knowledge about variabilities among device modeling experts, characterization experts and designers. The task is further complicated by the fact that different domain experts have different expectations on the variability models.

4. Acknowledgement

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5. Looking Forward

Based on the feedbacks of the workshop attendees and our sponsors, it is clear that the variability challenges we are facing requires collaboration among experts of multiple domains. There is still a unique need to bring them all together, so that meaningful dialog can happen among those communities. If condition permits, we are planning to continue this workshop with further fine-tuning next year.