Abstract

1. Atomistic Level Variations
   - Atomistic Simulation of Variability (Scott Roy/Glasgow)

     Abstract

     Device parameter fluctuations, which arise from both the stochastic nature of the manufacturing process and more fundamentally from the intrinsic discreteness of charge and matter, are a dominant source of device mismatch in nano-CMOS devices, and a bottleneck to the future yield and performance of circuits and systems. Fundamental sources of device variability such as; the random dopant distribution, lithographic line edge roughness, dielectric geometry and composition variations, other gate stake inhomogeneities and stress effects, will be described. Techniques for accurate and efficient physical simulation of these sources of variability will be discussed, and the need for simulation of variability out to at least 6σ from the mean stressed. Finally, methods of introducing the results of device variability simulations efficiently into compact model cards and ECAD tools will be suggested.

   - Nanoscale Transistor Design Optimization in Consideration of Atomistic Effects (Tsu-Jae King Liu /UCB)

     Abstract

     Random variations in threshold voltage (Vth) due to atomistic effects are projected to grow rapidly as gate lengths are scaled down below 25nm in sub-22nm bulk CMOS technologies. This will impose a limit on voltage scaling, which presents a serious problem for transistor density scaling. This presentation will discuss the benefits of advanced transistor structures for mitigating this issue, and how atomistic effects will affect their design optimization.

   - Study on Variability in Transistor Characteristics due to Random Telegraph Noise (Naoki Tega/Hitachi America)

     Abstract

     Random telegraph noise (RTN) arises from the trapping and detrapping of carriers at individual traps near the gate oxide interface, and then a threshold voltage variation (ΔV_{th}) is caused by RTN in FET. According to the RTN theory, the V_{th} variation is inversely proportional to device size, and therefore RTN potentially has an impact on scaling of digital devices with relatively-large noise margin. In the scaled FETs, the average number of traps causing RTN is less than one per FET. However complex RTN with multiple simultaneous trapping events is observed because traps are discretely distributed. In other words, large RTNs appear in scaled FETs even though they remain rare events. Therefore, the quantification of the impact of RTN on scaled FET requires not only an attention to typical RTNs but also the statistical analysis of RTN. In this talk, the impact of RTN on scaled FET using statistical analysis and the comparison in RTN V_{th} variation between nFET and pFET will be shown mainly.

2. Process Induced Variations
   - Topology Matters: When a Sensitive Circuit Meets Transistor Variation (Paul Newman/Intel)

     Abstract

     One can minimize the effects of transistor variation on circuit response by using robust topologies. Two examples of good and bad topologies are presented: a Front Side Bus input amplifier and a register file memory cell.

- Revisiting Variation Models and their Reliability (Puneet Gupta/UCLA)
  Abstract
  In this talk, we discuss and revisit (1) origins and physically justifiable modeling of spatial variation; and (2) confidence in statistical variation models. We analytically study the impact of across-wafer variation and show how it gives an illusion of correlation. We have developed a new die-level spatial variation model and show that our model is within 1% error from exact simulation result while the error of the existing distance-based spatial correlation model is up to 8% (despite being as much as 10X slower). Secondly, we study statistics of statistics. We shod that due to limited number of samples
  (especially in the case of lot-to-lot variation), calibrated models have low degree of confidence. The problem is further exacerbated when production volumes are low (< 65 lots) (since production only sees a small snapshot of the entire distribution). Our experiments (with variability assumptions derived from test silicon data from a 65nm industrial process) indicate that for moderate characterization volumes (10 lots) and low-to-medium production volumes (15 lots), a significant guardband (e.g., 34.7% of standard deviation for single parameter corner, 38.7% of standard deviation for SPICE corner, and 52% of standard deviation for 95%-tile point of circuit delay) is needed to ensure 95% confidence in the results.

- Modeling Layout-Induced Proximity Effects (Victor Moroz/Synopsys)\
  Abstract
  A distinction is given for random vs. systematic variability mechanisms and how they are accounted for. Physics of major layout-induced proximity effects, such as the stress effect, is described. Rule-based and model-based modeling approaches for systematic proximity effects are reviewed and an appropriate design flow is suggested.

3. Emerging parametric variations and extraction
   - Challenges of Predicting Product Level Degradation from Simple Device Level Models (Tanya Nigam/Global Foundries)
     Abstract
     In this talk, we will discuss the challenges of predicting product level degradation from device level models. A good correlation between the two requires a detailed understanding of the physical mechanisms which govern the different modes of degradation and some basic understanding of circuit functionality. Detailed modeling for HCI and BTI will be discussed and its impact on RO will be shown.

   - Efficient Techniques for Variation-Aware Electrical Modeling and Verification of VLSI Interconnect (Abe Elfadel/IBM)
     Abstract
     In this presentation, we survey the sources of geometric variabilities in VLSI interconnect, including lithography, CMP, and etch-dependent biasing. We then introduce simple, context-aware methods for evaluating the impact of interconnect width biasing on its RC model and show some of the limitations of such methods. We then illustrate the importance of computing the sensitivities of resistances and capacitances with respect to geometric variabilities if we are to rigorously develop variation-aware wire models or implement variation-aware parasitic extraction flows. We survey some of the progress made recently for the efficient computation of resistance and capacitance sensitivities using both mesh-based and mesh-less techniques. Finally, we show how these techniques are integrated and used in the context of a variation-aware parasitic extraction flow for VLSI layouts.

- Virtual Probe: Minimum-Cost Silicon Characterization of Nanoscale Integrated Circuits (Xin Li/CMU)
  Abstract
  We propose a new technique, referred to as virtual probe (VP), to efficiently measure, characterize and monitor both inter-die and spatially-correlated intra-die variations in nanoscale manufacturing process. VP exploits recent breakthroughs in compressed sensing to accurately predict spatial variations from an exceptionally small set of measurement data, thereby reducing the cost of silicon characterization. By exploring the underlying sparse structure in (spatial) frequency domain, VP achieves substantially lower sampling frequency than the well-known (spatial) Nyquist rate. In addition, VP is formulated as a linear programming problem and, therefore, can be solved both robustly and efficiently. Our industrial measurement data demonstrate that by testing the delay of just 50 chips on a wafer, VP accurately predicts the delay of the other 219 chips on the same wafer. In this example, VP reduces the estimation error by up to 10x compared to other traditional methods.

4. Characterization of Device and Circuit Variability
   - Challenges of designing robust physical IP in nanoscale CMOS technologies (Vikas Chandra/ARM)
     Abstract
     As we move into the sub-32nm era, the design of robust physical IP becomes increasingly challenging. Without substantial improvement in lithography capabilities, sub-32nm designs become heavily constrained by fundamental printing issues and increased variability. Since a physical IP library is developed quite early in the process maturity curve, the uncertainty in models creates a further challenge. Various test structures are often fabricated early in the process to correlate silicon with the models. However, in practice, there are various issues in correlating the two due to the increasing overlap of defect and variability spread. In this talk, I will discuss few of these challenges and explain our methodology to design a high-performance physical IP in nanoscale technology nodes.

   - In-situ Characterization of SRAM Variability (Lawrence Clark/ASU)
     Abstract
     Measurement and extraction of as fabricated SRAM cell variability is essential to process improvement and robust design. This is challenging in practice, due to the complexity in the test procedure and requisite numerical analysis. This talk reviews existing on-die SRAM margin measurements and proposes a new test structure and procedure for SRAM cell write margin measurement. The structure and approach are amenable to integration in to production die. Methods to extract transistor threshold voltage (V_{TH}) variations from the measurements, allowing accurate determination of SRAM cell stability are also discussed. The approaches are demonstrated with 90 nm test chips. The advantages of the proposed structure and method include: SRAM test structures with no disturbance to normal SRAM operations; a simple test procedure that only requires quasi-static control of external voltages; and methods to directly extract the V_{TH} variation of each transistor from measurements.

   - On-Chip Reliability Monitors: Circuit Ideas, Measurements and Limitations (Chris Kim/U Minnesota)
     Abstract
     The parametric shifts or circuit failures caused by Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Time Dependent Dielectric Breakdown (TDDB) have

become more severe with shrinking device sizes and voltage margins. These mechanisms must be studied in order to develop accurate reliability models, which are used to design robust circuits. Another option for addressing aging effects is to use on-chip reliability monitors that can trigger real-time adjustments to compensate for lost performance or device failures. The need for efficient technology characterization and aging compensation is exacerbated by the rapid introduction of process improvements, such as high-k/metal gate stacks and stressed silicon, which lead to a variety of new reliability issues. In this talk, I will introduce a number of unique test chip designs that we have implemented in order to demonstrate the benefits of utilizing on-chip digital circuits and a simple test interface to automate aging experiments.