Test Structures, Circuits, and Extraction Methods for Determining Pattern Density Effects

Duane Boning/MIT

Abstract: In advanced CMOS processes, variations in device performance can arise due to interactions between the designed device and other devices and structures in the "neighborhood" of that device. We discuss test structures, circuits, and extraction methods to detect and separate pattern density related effects at multiple length scales. At short distances, the local layout of the device together with nearest neighbors can have a strong impact on device performance (e.g., Idsat). Medium and longer range pattern density effects can also exist. We describe a test chip design focused on identification and extraction of local and medium-range poly and STI pattern density effects. A new test chip, with 130k devices under test (DUTs) and step-like pattern density layout changes, is designed in 65nm technology as a case study. The extraction result of the measured data suggests that the strongest effect arises within a radius of influence within the DUT cell size of 6um x 8um. For this technology, local layout geometry is the main contributor to systematic device variation. Model and correlation-maximization based methodologies are explored to identify and quantify medium and longer range pattern density effects. In this case study, we find a long-range (greater than 1mm) interaction distance that is statistically significant, but small in magnitude. The test structure, circuit, and extraction methodologies presented here can help guide design rule generation strategies.

Biography: Duane Boning is Professor of Electrical Engineering and Computer Science at MIT. His degrees are also from MIT, including the Ph.D. in 1991. His research focus is variation modeling, control, and environmental issues in semiconductor and MEMS manufacturing, with emphasis on chemical mechanical polishing and plasma etch, and CAD tools for statistical process, device, and circuit design. He has over 120 papers and conference presentations in these areas of research. From 1991 to 1993 he was a Member of the Technical Staff at Texas Instruments in Dallas. He served as the Associate Director for the MIT Microsystems Technology Laboratories from 1998 to 2004. He is a Fellow of the IEEE, for contributions to modeling and control in semiconductor manufacturing. He is currently Associate Head for Electrical Engineering in the EECS Department at MIT, and is the Editor in Chief of the IEEE Transactions on Semiconductor Manufacturing.

Improving Design, Manufacturing, and Even Test through Test-Data Mining

Shawn Blanton/CMU

Abstract: Since yield is not 100%, the main objective of test has and continues to be screening out bad ICs. Today, however, test is being used to provide valuable information about failing chips, answering questions about whether the design, the fabrication process or some combination of the two is responsible for failure. The information extracted is, ideally, used to improve design, fabrication and even test itself. In this talk, an overview of our work in this area will be described with particular emphasis on two methodologies that focus on improving design and test using normally-available test data. Actual results from manufactured chips from LSI, IBM and Nvidia will be used to illustrate the capabilities of these approaches.

Biography: Shawn Blanton is a professor in the Department of Electrical and Computer Engineering at Carnegie Mellon University where he serves as director of the Center for Silicon

System Implementation (CSSI), an organization consisting of 18 faculty members and over 80 students focused on the design and manufacture of silicon-based systems. He received the Bachelor's degree in engineering from Calvin College in 1987, a Master's degree in Electrical Engineering in 1989 from the University of Arizona, and a Ph.D. degree in Computer Science and Engineering from the University of Michigan, Ann Arbor in 1995.

Professor Blanton's research interests include the verification, test and diagnosis of integrated, heterogeneous systems. He has published over 90 papers in these areas and has several issued and pending patents in the area of IC test and diagnosis. Prof. Blanton has received the National Science Foundation Career Award for the development of a microelectromechanical systems (MEMS) testing methodology and two IBM Faculty Partnership Awards. He is a Fellow of the IEEE, and is the recipient of the 2006 Emerald Award for outstanding leadership in recruiting and mentoring minorities for advanced degrees in science and technology.

Measurements and Post-Fabrication Self-Improvement of SRAM Cell Stability

Toshiro Hiramoto/Univ. of Tokyo

Abstract: We have designed and fabricated 16kb SRAM DMA-TEG. In the first half of the talk, the relationship between measured static noise margin (SNM) and V_{th} of individual transistors in SRAM cells is discussed. It is found that the SNM variability is not explained by measured V_{th} variability alone. In the second half, the post-fabrication self-improvement of SRAM cell stability is proposed and experimentally demonstrated. The cell unbalance is self-suppressed because V_{th} of the stronger transistor is automatically raised by BTI stress.

Biography: Toshiro Hiramoto received B.S., M.S., and Ph.D degrees in electronic engineering from the University of Tokyo in 1984, 1986, and 1989, respectively. In 1989, he joined Device Development Center, Hitachi Ltd., Ome, Japan. In 1994, he joined Institute of Industrial Science, University of Tokyo, Japan, and has been a Professor since 2002. His research interests include low power CMOS device design, variability, silicon nanowire transistors, and silicon single electron transistors.

The Impact of Process Variability as It Relates to Modeling and Design in Advanced CMOS Technologies

Brandt Braswell/Freescale

Abstract: The design of optimized integrated circuits, with high-yield and high-reliability, in sub-250nm CMOS technologies requires models and simulations tools that capture and accurately reflect the statistical variations and the physical attributes of the circuits.

Biography: My name is Brandt Braswell and I am an analog design engineer at Freescale Semiconductor. I started my career in the semiconductor industry in 1991 out of college. I worked for National Semiconductor in Santa Clara CA in the Custom Linear ASIC group from 1991-1995 at which time I accepted a job with Motorola and moved to Arizona to work in the radio group of the Semiconductor Product Sector - which later was sold and became Freescale Semiconductor.

I am married and have three wonderful kids. I find enjoyment in life and work by learning and associating with great friends and co-workers. I try to challenge my self at work and find reward

by finding answers to challenging problems. I try to keep in shape by attending the gym regularly and have fun camping and riding motorbikes.

Characterization and Modeling of MOSFET Noise in Sub-threshold Region

Debarshi Basu/TI

Abstract: With ever increasing motivation to improve power specification, there is considerable momentum for analog designs to operate the MOSFETs in sub-threshold or weak-inversion regions. Conversely, MOSFET noise is typically characterized in linear and/or strong-inversion saturation regions. This data is used create SPICE models. This approach brought into question the accuracy of the models in other operating regions, especially in sub-threshold. In recognition of the need for accurate noise modeling under those operating this presentation will discuss the applicability of the industry standard noise models in weak inversion and subthreshold regions. For noise sensitive analog application the statistical variation of flicker noise becomes important. Statistical noise variations observed in model will also be presented. Data from an analog technology at TI will be compared with SPICE model simulation.

Biography: Dr. Debarshi Basu is a SPICE modeling specialist at Texas Instruments. He has worked on modeling advanced CMOS as well as analog technologies at Texas Instruments. He has also worked as a consultant providing device modeling services for Fortune 500 technology companies worldwide. He received his PhD in Organic semiconductors with graduate portfolio in Nanotechnology from UT Austin in 2007. He also works as an application developer for android phones.

Handling Process Variability: Self-Testing and Self-Tuning Mixed-Signal/RF Circuits and Systems

Abhijit Chatterjee/GaTech

Abstract: Design and test of high-speed mixed-signal/RF circuits and systems is undergoing a transformation due to the effects of process variations stemming from the use of scaled CMOS technologies that result in significant yield loss. As a consequence, on-chip test, validation and tuning algorithms and support infrastructure need to be developed to allow low cost manufacture of complex SoCs. A novel signature-based test, validation and tuning paradigm is presented that allows rapid and accurate diagnosis of system-level model parameters. The method allows the design of efficient built-in test mechanisms as well as facilitates post-silicon validation of complex AMS/RF systems. A further benefit is the ability to tune complex AMS/RF systems using iterative tuning algorithms. The key test challenges are discussed and promising solutions are presented in the hope that it will be possible to design, manufacture and test truly self-healing systems in the future.

Biography: Abhijit Chatterjee is a Professor in the School of Electrical and Computer Engineering at Georgia Tech and a Fellow of the IEEE. He received his Ph.D in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. Chatterjee received the NSF Research Initiation Award in 1993 and the NSF CAREER Award in 1995. He has received four Best Paper Awards and three Best Paper Award nominations. In 1996, he received the Outstanding Faculty for Research Award from the Georgia Tech Packaging Research

Center, and in 2000, he received the Outstanding Faculty for Technology Transfer Award, also given by the Packaging Research Center. Chatterjee has published over 340 papers in refereed journals and meetings and has 12 patents. He is a co-founder of Ardext Technologies Inc., a mixed-signal test solutions company and served as Chairman and Chief Scientist from 2000 - 2002. He is currently directing research at Georgia Tech in mixed-signal/RF design and test funded by NSF, SRC, MARCO-DARPA and industry.

New Sources of Variability in 3D TSS Technologies

Riko Radojcic/Qualcomm

Abstract: This presentation provides an overview of a through-si-via based 3D stacking technology and identifies sources of variability that are incremental to those found in typical 2D advanced CMOS technologies. The intimacy of the die-to-die interactions enabled by 3D stacking, as well as the introduction of new features (eg TSV) and new processes (eg thinning) all precipitate new sources of variability and susceptibility, especially in thermal and mechanical stress domains. A concept design flow is outlined, and the philosophy of the methodologies to address the new sources of variability within this design flow is proposed.

Biography: Riko Radojcic is a Director of Engineering at Qualcomm CDMA Technologies, and a leader of various Design-for-Technology initiatives; including Design for 3D Integration, design for Manufacturability & Variability, Si-package CoDesign, etc., and involving methodologies at polygon, circuit, logic, and/or system design levels.

Radojcic has more than twenty-five year's experience in the semiconductor industry, specializing in the integration of process, design and EDA considerations, and design-for-Si solutions. Before joining Qualcomm, he was a consultant to semiconductor and EDA companies providing engineering and business development services focused on process-design integration. He was a director of business development and marketing for DFM solutions at PDF Solutions and was a business manager and an architect with Tality and Cadence, specializing in design technology integration and process characterization and modeling.

Radojcic has held a series of managerial and engineering positions with Unisys and Burroughs, in device engineering, failure analyses and reliability engineering areas. He began his career as a process engineer with Ferranti Electronics, UK.

Radojcic received his BSc and PhD degrees from University of Salford, UK.

Managing Variability in 3D IC

Paul Franzon /NCSU

Abstract: Variability in 3DIC will manifest itself as increased variation between different chips in the stack and unique variations induced through additional process steps. The former can be managed through design, particularly appropriate circuit partitioning even in aggressive highly disaggregated systems. The latter requires a DFM approach that is numerically predictive in nature.

Biography: Paul D. Franzon is currently a Professor of Electrical and Computer Engineering at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Adelaide, Australia in 1988. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia

Telecom and two companies he cofounded, Communica and LightSpin Technologies. His current interests center on the technology and design of complex systems incorporating VLSI, MEMS, advanced packaging and nano-electronics. He has lead several major efforts and published over 180 papers in these areas. In 1993 he received an NSF Young Investigators Award, in 2001 was selected to join the NCSU Academy of Outstanding Teachers, in 2003, selected as a Distinguished Alumni Professor, and in 2005 won the Alcoa award. He is a Fellow of the IEEE.

Interconnect Networks in 2D and 3D Nanoelectronic Systems

Azad Naeemi/GaTech

Abstract: In this talk, an overview of interconnect limitations in many-core chips implemented in future technology nodes will be presented. The talk will cover within core interconnect issues as well as network-on-chip (NoC) interconnects for core-to-core communication. It will be shown that wiring demand and the impact of interconnect variability highly depends on the network topology. Finally, 2D and 3D networks will be compared and discussed.

Biography: Azad Naeemi received his Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, in 2003. He worked as a Research Engineer with the Microelectronics Research Center, Georgia Tech, from 2003 to 2008 and has been an Assistant Professor with the School of Electrical and Computer Engineering, Georgia Tech, since 2008. His areas of interest include performance modeling for conventional and emerging interconnect technologies, interconnects for post-CMOS devices, and system-level evaluation of potential nanoelectronic devices and interconnects.

Dr. Naeemi is a member of the International Technology Roadmap for Semiconductors technical working group on Interconnects. He has received a Semiconductor Research Corporation Inventor Recognition Award and is the recipient of the IEEE Electron Devices Society (EDS) Paul Rappaport Award for the best paper that appeared in IEEE Transactions on Electron Devices in 2007.

TSV Stress Effects for Digital and Analog Circuits

Victor Moroz/Synopsys

Abstract: Overview of TSV induced stress is given for several alternative TSV process options. The impact of TSV on analog and digital transistors is quantified for single TSV, TSVs arranged in rows, and TSVs arranged in matrices. The worst case scenario has keep-out zone of 200 microns. Appropriate keep-out zones and design rules are proposed for different TSV arrangements and circuit types.

Biography: Victor Moroz received his Ph.D. in Semiconductor Physics in 1992 from the University of Nizhny Novgorod, Russia. His professional career revolves around semiconductor physics and includes silicon process integration in the industry, teaching undergraduate and graduate students, and for the last 15 years - developing TCAD tools and modeling methodologies at TMA and TCAD Department at Synopsys. Several facets of this activity are reflected in a book and over 100 technical papers, invited presentations, and patents. Currently serving on technical committees at IEDM, ESSDERC, and ITRS.