Posters

1. A Transistor-array for Parallel BTI-effects Measurement
   Takumi Uezono, Tadamichi Kozaki, Hiroyuki Ochi, and Takashi Sato/Kyoto Univ.
   A novel test structure, which facilitates efficient measurement of threshold voltage (Vth) variation and degradation caused by bias temperature instability (BTI) effects, is proposed. The proposed structure consists of a device array with individual bias control module. The bias control module changes the connections of device-terminals to voltage sources so that a different status such as stress, recovery, or measurement is selected for each device. The proposed array makes it possible to measure Vth of a device while undergoing stresses to other devices in the background. The proposed structure is useful to characterize the BTI-induced Vth shift for a large number of devices.

2. Buffer-Ring-Based All-Digital On-Chip Monitor for PMOS and NMOS Process Variability Measurement
   Tetsuya Iizuka, Jaehyun Jeong, Toru Nakura, Makoto Ikeda, and Kunihiro Asada/Univ. of Tokyo
   This paper proposes an all-digital on-chip monitor for PMOS and NMOS process variability utilizing a simple buffer ring with a pulse counter.
   The proposed circuit monitors the process variability according to a count number of a single pulse which propagates on the buffer ring and a fixed logic level after the pulse disappears. The proposed circuit has been fabricated in 65nm CMOS process and the measurement results demonstrate that we can monitor the PMOS and NMOS variabilities independently using the proposed monitoring circuit.

3. Digital Circuit Simulation with Random Telegraph Noise
   Yun Ye, Chi-Chao Wang, Yu Cao/ASU
   With the continuous reduction of CMOS device dimension, the importance of discrete Random Telegraph Noise (RTN) keeps growing up. To determine its impact on circuit performance and optimize the design, it is essential to physically model RTN effect and embed it into standard simulation environment. In this paper, a new simulation method of time domain RTN effect is proposed to benchmark important digital circuits:
   (1) A two-stage L-element sub-circuit is proposed to generate RTN signal by integrating a white noise source. An L-element is a RC filter connected with an ideal comparator, where RC values are calibrated with the physical property of RTN.
   (2) This sub-circuit is fully compatible with SPICE. It successfully reproduces the discrete RTN signal, enabling the time domain analysis scaled digital design;
   (3) The importance of discrete RTN is demonstrated on a 32nm SRAM design and a 22nm low power ring oscillator (RO), using the proposed method. As compared to traditional 1/f noise, the impact of RTN is more significant under low voltages, leading to tremendous differences in the prediction of V_{ccmin} and failure probability in SRAM, as well as jitter noise in RO.

4. Effect of the Channel Dopant Non-Uniformity on V_{TH}-Variation
   Kazuo Terada, Kazuhiko Sanai, Katsuhiro Tsuji, Takaaki Tsunomura, Akio Nishida and Tohru Mogami/Hiroshima City Univ.
   MOSFET threshold-voltage (V_{TH}) variation is affected by not only the channel area but also the channel dopant non-uniformity.
   Using the test devices, which include many MOSFETs having various channel width (W) and length (L), the effects of channel dopant non-uniformity are measured. It is found that the random V_{TH}-variation component, which is independent of 1/ LW, exists and it should be considered in the design.

5. Evaluation of Delay Variation and Soft-Error Hardness in Asynchronous Pipeline Circuits
   Masashi Imai and Tomohiro Yoneda/Univ. of Tokyo
   As the VLSI technology advances, it has been recognized that delay variations become extremely large. Asynchronous circuits which tolerate delay variations are going to be recognized as a feasible solution to the timing-related problems. On the other hand, it is pointed out that asynchronous circuits are sensitive to glitches due to soft errors, which become serious problems in the scaled CMOS technologies.
   In this poster, we discuss the problems and solutions of soft errors in asynchronous circuits. We show some evaluation results of delay variations and soft-error tolerance techniques in asynchronous pipeline circuits.

6. Modeling of Random Telegraph Noise under Circuit Operation – Simulation and Measurement of RTN-induced Delay Fluctuation:
   Kyosuke Ito, Takashi Matsumoto, Shinichi Nishizawa, Hiroki Sunagawa, Kazutoshi Kobayashi, and Hidetoshi Onodera/Kyoto Univ.
   In this poster, we discuss the impact of Random Telegraph Noise (RTN) on delay of combinatorial circuits. We have measured RTN-induced delay fluctuation using a circuit matrix array fabricated in a 65nm process. We have also developed an RTN-aware delay model based on Markov process with RTN statistical property. From comparison between measured and simulated delay fluctuations data, we indicate the unique RTN-behavior under circuit operation. Based on the RTN-aware delay model , the impact of RTN in future scaled technologies is discussed.

7. On-chip In-situ Measurements of V_{th}, Signal Gain, and Substrate Sensitivity of Differential Pair Transistors
   Satoshi Takaya, Yoji Bando*, Toru Ohkawa+, Toshiharu Takaramoto+, Toshio Yamada+, Masaaki Souda+, Shigetaka Kumashiro+, Tohru Mogami+, Makoto Yamada+Nagata*/*Kobe University, +MIRAI-Selete, Japan*
   In-situ measurements of AC signal gain (Gsig) and AC substrate sensitivity (G_{sub}) of differential pair transistors in an analog amplifier use on-chip continuous time waveform monitoring. In addition, threshold voltage (V_{th}) of the same transistors is derived through

DC measurements in combination with an off-chip semiconductor parameter analyzer. Design of a test structure for measuring these quantities of transistors in an analog circuit and relevant evaluation to the variability in analog devices will be discussed.

The test structure of [1] is expanded for the evaluation of signal gain and substrate sensitivity of transistors in a differential pair. It is developed with on-chip continuous-time monitors of [2] and forms a matrix of amplifiers featuring on-chip in-situ measurements of DC characteristics and AC response of the transistors.

A prototype chip for 1.0-V transistors in a 90-nm CMOS technology demonstrates the distribution of AC gain versus DC Vth of transistors within amplifiers. It also derives the relation of Gsig and Gsub as well. The degradation of common-mode rejection property is observed for an amplifier with intentionally introduced mismatches to the pair of transistors.

8. Statistical Delay Estimation with Path-Delay Test

Yasuhiro Takashima, Takanobu Shiki, and Yuichi Nakamura/Kitakyu Univ.

According to the improvement of the recent LSI construction process, the process variation becomes a critical issue. Especially, a timing error occupies 30% on fabricated chips defects. To solve the issue, it is very important to acquire the information and condition inside of fabricated chips.

If the information and conditions of chips could be obtained, the origin of the defects can be known easily, and the various recovery methods can be applied for the current fabricated chips [2] and the next fabrication chips [3].

However, it is very expensive and complicated to obtain the inside information and condition of fabricated chips, especially the propagation delays.

The well-known conventional methods are by using delay analysis circuits or measurement systems [2,4]. The delay analysis circuits can analyze accurate propagation delay values, since they can observe the delay in circuit at real time. The measurement system is connected to chip and can observe the propagation delay value from the outside of the chip. Both methods are very useful, however, they have large overhead. The delay analysis circuits increase the chip area, and the measurement system needs the extra external interface on the chip.

In this work, we employ the path-delay test with scan-FFs to obtain the path delay information. The path-delay test is usual for the at-speed test [5].

Thus, its estimation cost seems to be small enough. The result of path-delay tests indicates whether the tested path satisfies the timing constraint or not.

Thus, we consider that the delay of each tested path exists within some range after the tests. We assume that the probability distribution of each net is calculable and the probabilities of two nets are independent of each other.

We proposed the method for both the serial and the branch model [6, 7].

The serial model consists of several nets connected serially. On the other hand, the branch model is that several nets consist of a junction. Fig.1 shows both models.

To confirm the accuracy of the proposed method, we compared the values from our method and Monte-Carlo simulation. In the experiments, we assume that the probabilistic distribution of every net holds the normal distribution. From the experimental results, averages of errors of the proposed method from the result of Monte Carlo simulation are within 0.05%. Thus, we conclude the accuracy of the proposed method is enough.
We also applied our method to a small example shown in Fig.2. In this circuit, we tested the path-delay tests for the paths FF1-FF2 and FF1-FF3, and we estimated the delay value of the path FF1-FF4 according to the test results. To compare Monte Carlo result, the errors are within 0.005%. Thus, we confirm our model and calculation to be correct.

9. Statistical Thermal Evaluation and Yield Improvement Considering Process Variation for 3D Chip-Multiprocessor
   Da-Cheng Juan, Siddharth Garg and Diana Marculescu/CMU
   Thermal issues have become critical roadblocks for achieving highly reliable three-dimensional (3D) integrated circuits. The presence of process variations further deteriorates these problems. This paper performs both the evaluation and mitigation of the impact of leakage power variations on the temperature profile of 3D Chip-Multiprocessors (CMPs). Furthermore, this paper provides a learning-based model to predict the maximum temperature, based on which a simple, yet effective tier-stacking algorithm to mitigate the impact of variations on the temperature profile of 3D CMPs is proposed and evaluated. Results show that (1) the proposed prediction model achieves more than 98% accuracy, (2) a 4-tier 3D implementation can be more than 40oC hotter and 23% leakier than its 2D counterpart and (3) the proposed tier-stacking algorithm significantly improves the thermal yield from 44.4% to 81.1% for a 3D CMP.

10. The Area Criteria of 6T and 8T SRAM Cells
    Shusuke Yoshimoto, Shunsuke Okumura, Hiroshi Kawaguchi and Masahiko Yoshimoto/Kobe Univ.
    This poster shows criteria for selecting 6T or 8T SRAM cells in terms of bitcell area. As a CMOS process technology is scaled down, threshold voltage variation is increased. In particular, degradation of operating margins (both of read and write margins) in an SRAM memory cell becomes a serious problem. To suppress the degradation and improve the operations at a low voltage, the classic 6T cell size tends to be larger with the advanced processes. On the other hand, the 8T cell equipped with a separate read port needs write margin only. Therefore the 8T cell will be smaller than the 6T cell in a quite large-capacity SRAM (at 6 sigma Vth) in a future process. However, the large capacity SRAM with the state-of-the-art process does not be always needed for designers. The area advantage between 6T and 8T cell depends on the specific restricts: a process technology, a supply voltage, and a memory capacity. In this paper, a border between the 6T cell and the 8T cell is predicted as to the restricts. When the process is 32 nm and the supply voltage is 1.0 V, the 6T SRAM cell is larger than the 8T cell at 134 Kbit or more.

11. 3D Ensemble Monte Carlo Device Simulations of Random Trap Induced Degradation in Drain Current and in Threshold Voltage in the Presence of Random Dopant Distributions for 45 nm Gate

    Nabil Ashraf, Dragica Vasileska/ASU

    We investigate the influence of a single trap and two traps in close proximity located at the semiconductor/oxide interface (positioned in the middle portion of the gate width and gradually moved from the source end to the drain end of the channel). We find that when the trap is located at the source end of the channel, the threshold voltage and the magnitude of the drain current are dominated by the potential barrier created by the negatively charged (repulsive) trap. When the trap is positioned at the drain end of the channel, the barrier effect on carrier transport is smaller and screening (for small drain bias) and the absence of screening (at large drain bias due to the presence of pinch-off region) determine whether current will not be degraded or will be degraded, respectively. Additionally, the simulations reveal that the degradation characteristics are worse for the case of two traps in close proximity when compared to a single trap case at the same relative trap position because two traps in close proximity generate higher Coulomb potential barrier in the vicinity of the trap's interaction zone with the carriers, impending transport of carriers in the channel from source to drain region of the MOSFET. Twenty random dopant configurations are used for each trap position. We find that this size of the statistical sample is sufficient to give reliable and physically meaningful results.

12. Variation Characterization for Morphic Circuits in Multi-core Interconnects

    Ravi Kiran B Raghavendra , Fahd Shaikh, Sun Jin, Janet Roveda/Univ. of Arizona

    Variations, as seen in the IC industry are a crucial challenge. With the advent of Multi-core architectures, one fundamental question is how to provide adaptive connections among cores. As a corner stone of this fundamental research, in this project, we provide characterizations for morphic circuits that are used for inter-core connections. One key aspect that we can thrive on is the topology for these structures. Previous work has shown that there is no single topology that is optimal for all the applications [1]. Thus there is a scope for varying the topology to get the best out of the available resources. Our idea in doing this research is to find a way to change the topology of the multi-core architecture depending on the application, before runtime. We believe that these morphic circuits will have difference variability properties. And the models of these morphic circuits will provide keys to an optimal performance/delay/power/BER for the system. Further, there is another area that can be exploited to optimize the design. Network designers had always faced a tough situation in picking among "circuit switch network" or "packet switch network" [2], [3]. In this work we would like to add this extra design parameter to optimize the metrics. Overall, we have a morphic structure that would change the topology and the switching scheme basing on the application.