Posters

1. $g_m$ Variability Caused by Local Threshold-Voltage Fluctuation
   
   K. Terada, R. Takeda and K. Tsuji / Hiroshima City University

2. Reliability Studies in 45 nm Technology node: Threshold Voltage Fluctuations due to Random Dopants and Random Telegraph Noise
   
   N. Ashraf, S. Joshi and D. Vasileska / Arizona State University

3. Transistor Array Layout-style with Channel Length Decomposition for Analog Designs
   
   B. Yang, B. Liu, G. Chen, L. Jing, Q. Dong, T. Fujimura and S. Nakatake / University of Kitakyushu

4. VAREX: A Post-P&R Variability Modeling Framework for Multiprocessor SoCs
   
   M. Montazpour, O. Assare, H. I. Rad, M. Goudarzi, E. Sanaei / Sharif University of Technology

5. Nanosized-Metal-Grain-Induced Characteristic Fluctuation in 16-nm-Gate FinFET Device with TiN/HfO2 Gate Stack and Digital Circuits
   

   
   K. Qian, Y. Qiao and C. J. Spanos / University of California, Berkeley

7. Impact of RTN and NBTI on Synchronous Circuit Reliability
   
   T. Matsumoto, K. Kobayashi and H. Onodera / Kyoto University

   
   M. Shintani and T. Sato / Kyoto University

9. Variation of Substrate Sensitivity in Differential Pair Transistors
   
   S. Takaya, T. Hasegawa, Y. Bando, T. Ohkawa, T. Takaramoto, T. Yamada, M. Souda, S. Kumashiro, M. Nagata / Kobe University

10. Analysis on PVT Resilience and Dependable Low Voltage Operation of Self-Synchronous FPGAs
    
    M. Ikeda, B. Devlin / University of Tokyo

    
    J. B. Velamala, T. Sato, Y. Cao / Arizona State University

12. Using Parametric OCV to Improve Timing Closure
    
    B. Cline, A. Mutlu / ARM

    
    R. Garg, S. Garg / University of Waterloo