Posters

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5. Nanosized-Metal-Grain-Induced Characteristic Fluctuation in 16-nm-Gate FinFET Device with TiN/HfO2 Gate Stack and Digital Circuits
   H.-W. Cheng, Y. Li, C.-Y. Yiu and H.-W. Su / National Chiao Tung University
6. Statistical Compact Model Characterization for Variability-Aware Circuit Design Optimization
   K. Qian, Y. Qiao and C. J. Spanos / University of California, Berkeley
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10. Analysis on PVT Resilience and Dependable Low Voltage Operation of Self-Synchronous FPGAs
    M. Ikeda, B. Devlin / University of Tokyo
11. Statistical Aging Prediction and Characterization using Trapping/Detrapping based NBTI Models
    J. B. Velamala, T. Sato, Y. Cao / Arizona State University
12. Using Parametric OCV to Improve Timing Closure
    B. Cline, A. Mutlu / ARM
13. Modeling the Impact of Density Variations on Carbon Nanotube FET Based Digital Circuits
    R. Garg, S. Garg / University of Waterloo