

Posters

1. Including Variability in Simulation of Logic Circuits
Kevin Cameron, Cameron EDA
2. A Temperature and Process Variation Insensitive PDE Circuit Employing Neuron-MOS
Renyan Zhang and Mineo Kaneko, Japan Advanced Institute of Science and Technology
3. Optimal selection of measurements for statistical transistor compact model extraction
Li Yu, Ibrahim Elfadel, Dimitri Antoniadis and Duane Boning, MIT, *Masdar Institute*
4. Variability Analysis of Logic Cell Performance in 16nm
Takeshi Okagaki, Yasumasa Tsukamoto, Hiroaki Matsushita, Koji Shibutani and Koji Nii, Renesas Electronics Corp.
5. Characterization of sub-ppm delay outliers using 512K flip-flop ring oscillator test chip
Masaki Shimada, Kan Takeuchi, Hiroaki Matsushita, Hironori Sakamoto and Masahiro Ikeda, Renesas Electronics Corp.
6. Clock Skew Post-silicon Tuning by Multilevel Delay Locked Loop
Daijiro Murooka, Yu Zhang, Qing Dong and Shigetoshi Nakatake, The University of Kitakyushu
7. Layout-dependent Manufacturability Evaluation of Instrumentation Amplifier
Takuya Hirata, Ryuta Nishino, Shigetoshi Nakatake and Masaya Shimoyama, The University of Kitakyushu, *University of Miyazaki*
8. A Family of Ling Based Fault Tolerant Adders
Syed Ershad Ahmed, Abhilash Srinivasan, Edwin Anthony and Srinivas M.B, BITS-Pilani
9. Estimation of Within-Die and Die-to-Die CMOS Variability Based on Ring Oscillators
Juan Pablo Martinez Brito, Hamilton Klimach and Sergio Bampi, Federal University of Rio Grande do Sul - UFRGS
10. A Lognormal Timing Model and Design Guidelines for Near-Threshold Circuits
Jun Shiomi, Tohru Ishihara and Hidetoshi Onodera, Kyoto University
11. Initial Frequency Degradation and Variation on Ring Oscillators from Plasma Induced Damage in Fully-Depleted Silicon on Insulator Process
Ryo Kishida, Azusa Oshima, Michitarou Yabuuchi and Kazutoshi Kobayashi, Kyoto Institute of Technology
12. Reliability-Driven Testing of Digital Microfluidic Biochips
Zipeng Li, Tsung-Yi Ho and Krishnendu Chakrabarty, Duke University, *National Chiao Tung University*