VMC'15 Posters

1 Daisuke Kanemoto and Makoto Ohki, *"A CT Delta-Sigma Modulator Design Technique with Equivalent Gain of Multi-bit ADC Having Random Offset Voltages due to Device Mismatch."*

2 Hiromitsu Awano and Takashi Sato, *"Fast Monte Carlo for Timing Yield Estimation via Line Sampling."*

3 Ahmed Awad, Atsushi Takahashi and Chikaaki Kodama, *"A Fast Lithographic Mask Manufacturing Cost Aware Optical Proximity Correction (OPC) Algorithm With Process Variability Consideration."*

4 Jun Shiomi, Tohru Ishihara and Hidetoshi Onodera, *"Slew- and Variability-Aware Logical Effort for Near-Threshold Circuit Design."*

5 Chi-Hsuan Kao, Zih-Hong Yang, Cheng-Lan Huang, Yu-Sian Chang, Chung-Wei Wu, Ting-Yu Shyu, Pei-Yuan Chou, Tay-Jyi Lin and Jinn-Shyan Wang, *"Characterization of Delay Variations in Modern FPGAs."*

6 Mahfuzul Islam, Tetsuya Nakai and Hidetoshi Onodera, *"Characterization of Gate Width Dependency on Random Telegraph Noise using Reconfigurable Ring Oscillator for Compact Statistical Modeling."*

7 Tianshi Wang, Aadithya Karthik, Bichen Wu and Jaijeet Roychowdhury, *"MAPP: The Berkeley Model and Algorithm Prototyping Platform."*

8 Marco Donato and Iris Bahar, *"A Fast Simulator for the Analysis of Sub-Threshold Thermal Noise Transients."*