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Mehmet Meric Isgenc, Samuel Pagliarini, Mayler Martins and Larry Pileggi. **Exhaustive DFM Evaluation of Logic Cell Libraries via Virtual Characterization**

Shogo Yamaguchi, Hitoshi Imi, Shogo Tokumaru and Kazuyuki Nakamura. **Vth-shiftable SRAM Cell TEGs for Direct Measurement for the Immunity of the Threshold Voltage Variability**

Hongge Chen, Duane Boning and Zheng Zhang. **Efficient Spatial Variation Characterization via Matrix Completion**

Chiao-Chuan Huang, Hsin Yang, Ting-Yu Shyu and Tay-Jyi Lin. **Timing Margin Prediction for Energy-Efficient and Variation-Resilient Adaptive Voltage Scaling in Microprocessor Designs**

Xinfei Guo and Mircea Stan. **Enabling Wearout-Immune BEOL and FEOL with Active Rejuvenation**

Michihiro Shintani, Kazuki Oishi, Rui Zhou, Masayuki Hiromoto and Takashi Sato. **Unique Device Identification Framework for Power MOSFETs Using Inherent Device Variation**

Shumpei Morita, Song Bian, Michihiro Shintani, Masayuki Hiromoto and Takashi Sato. **Representative Path Approach for Time-Efficient NBTI Mitigation Logic Replacement**