VMC'17 Posters

1. Chao Geng, Bo Liu and Shigetoshi Nakatake (U. of Kitakyushu) — *Density-feasible Configuration of Transistor-array for Analog Layouts*
2. Ryota Tsuchihashi, Komei Nomura, Yasuhiro Takashima and Yuichi Nakamura (U. of Kitakyushu & NEC) — *Task allocation and scheduling optimization in the heterogeneous core system*
3. Taisei Kubo, Daijiro Murooka, Yasuhiro Takashima and Shigetoshi Nakatake (U. of Kitakyushu) — *Dynamic Clock Skew Adjustment by Multilevel Delay Locked Loop and its Variability Analysis*
4. Mohsen Imani, Abbas Rahimi, Deqian Kong, Tajana Rosing and Jan Rabaey (UC San Diego & UC Berkeley) — *Brain-Inspired Hyperdimensional Computing*
5. Mahfuzul Islam and Hidetoshi Onodera (U. of Tokyo and Kyoto University) — *Supply Voltage Effect on Random Telegraph Noise Induced Delay Variation*
6. Michihiro Shintani, Masayuki Hiromoto and Takashi Sato (NAIST & Kyoto University) — *Parameter Extraction for MOSFEET Current Model Using Backward Propagation of Errors*