

# Analysis of Power Supply Grid of Microprocessors

**Sandip Kundu**

Assumptions used in circuit design are often different from silicon reality. On top of this foundation, CAD tools must make approximations to handle increasingly bigger designs. When real silicon differs from "virtual" silicon used in design, a number of issues may arise including yield problems, shipped product quality problems and even product recall in extreme cases. Sandip started Circuit Marginality Test group at Intel to work on developing circuit marginality failure models to better target the pattern development process to expose these issues. In this talk, Sandip will introduce the problem, present relevant data and delve into one of the causes: power delivery to the transistors. He will present modeling approaches for analyzing power supply grid and how it responds to switching circuits. The solution is scalable to chips with billions of transistors.

**Bio:** Sandip Kundu is a Principal Engineer at Intel. He has published more than 50 papers in diverse areas including VLSI design, Testing, CAD and Coding & Information Theory. Sandip holds several patents, given more than 10 tutorials at conferences and served in program committees of all major CAD conferences (DAC, ICCAD, DATE and ASP-DAC). He was the Technical Program Chair of ICCD in 2000 and General Chair in 2001. He will serve as General Chair of VLSI 2005 conference. Sandip is currently an associate editor of IEEE Transactions on Computers.