

UT VLSI SEMINAR SERIES

Routing Interconnect and Future Scaling Issues

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ABSTRACT

Historically routing interconnect has been very slowly changing. Over the past 30 years interconnect has improved ~50X while during the same period transistor improvement is on the order of 1000X. Thus interconnect is becoming a dominate issue in performance improvement. The historical changes will be examined, the future problems will be examined and proposed directions will be discussed.

BIOGRAPHY

Jerry has over 30 years of experience in custom circuit design. Jerry is an AMD fellow and a Motorola Dan Nobel fellow. He designed DRAM's at Motorola from 1K to the 256K. He also designed some of the first EPROM devices of 8K and 16K devices. At AMD he headed up the 1Megabit DRAM activity and then took over the CMOS programmable logic group. In 1997 he moved into head up the custom design effort on K5 microprocessor group and headed up the K7 (Athlon) design effort.

Jerry has over 30 patents and had the most significant AMD patent award in 1999. He has presented one paper at the ISSCC and been on two panel discussions on DRAM's. Also he presented at the 2001 VLSI Symposium Workshop.