

# UT VLSI SEMINAR SERIES

## Floorplan Design for Complex VLSI Systems

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**4:30-5:30 PM**

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### ABSTRACT

Floorplanning tools, which determine the placement of all circuit blocks at each level of the hierarchy, play a crucial role in the divide-and-conquer solution to the layout of a complex VLSI chip. In this talk, we will present a floorplanner FAST-SP based on the sequence-pair (SP) floorplan representation. We present an  $O(n \log \log n)$  SP-to-floorplan translation algorithm based on longest common subsequence computation. Our algorithm is significantly faster than the traditional  $O(n^2)$  graph-based algorithm. It allows our simulated annealing based floorplanner to examine a larger number of candidate floorplans in shorter runtime and produce better quality floorplans. FAST-SP can also handle a large variety of placement constraints, and simultaneous block and bus planning.

### BIOGRAPHY

Dr. Wong is currently Professor of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign (UIUC). Before he joined UIUC, he was Professor of Computer Sciences at the University of Texas at Austin where he held a Bruton Centennial Professorship. He was on the CS faculty at UT-Austin from 1987 to 2002. Dr. Wong's research interests are CAD for VLSI, field-programmable systems, and combinatorial optimization. He has published over 250 technical papers and has graduated 29 Ph.D. students. Dr. Wong received the 2000 IEEE CAD Transactions Best Paper Award, best paper awards at DAC-86 and ICCD-95. His ICCAD-94 paper on circuit partitioning was included in the book "The Best of ICCAD - 20 Years of Excellence in Computer Aided Design" published in 2002.

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