

Defect-based Test for Defect Detection and Localization

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Abstract

Conventional VLSI testing methods are challenged by changing circuit sensitivities and emerging defect mechanisms resulting from the use of new fabrication materials in very deep submicron processes. For example, the change from a subtractive aluminum process to damascene Cu may lead to more particle-related blocked-etch resistive opens. Technology scaling also increases the probability of resistive vias caused by incomplete etch. The additional delays introduced by these types of resistive defects in combination with increased circuit sensitivity due to shorter clock cycles, reduced timing slack, crosstalk and PWR/GND bounce increase the likelihood of random defects causing delay fails. The power supply transient (I_{DDT}) and quiescent (I_{DDQ}) defect-based testing methods that we propose are designed to address these challenges, and others as given in the Test and Test Equipment section of the International Technology Roadmap for Semiconductors (ITRS). For example, ITRS specifies a need for novel defect-based methods to support the yield learning process, to replace I_{DDQ} and burn-in as reliability screens and to support non-destructive software based fault localization.

The novelty of our proposed methods lies in the measurement and joint analysis of multiple power supply pad signals. The power grids of many digital and SoC chips are interfaced to the external power supplies through multiple supply ports. We have determined that, much like the multiple output ports of digital logic provide a rich source of information concerning a chip's functional behavior, the same is true of the signals measured at each of the supply ports, with the added benefit that internal gate behavior is reflected in the temporal aspects of the measured signals. In previous work, we demonstrated the capabilities of our methods for detecting and localizing defects using simulations of a commercial power grid and a realistic power distribution system of a production test system. Our recent work is focused on hardware verification and the development of off-chip and on-chip signal measurement circuits. The techniques and recent hardware results will be presented.

Biography

Professor Plusquellic received the B.S. degree in Biology from Indiana University of Pennsylvania in 1983 and the M.S. and Ph.D. degree in Computer Science from the University of Pittsburgh in 1995 and 1997, respectively. He has recently been promoted to associate professor at the University of Maryland, Baltimore County. Professor Plusquellic is on the program committee for the International Test Conference and is program chair of the Defect Based Testing workshop at the VLSI Test Symposium. He is a member of both the IEEE and ACM.