



**THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES**



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Design of SEU-resilient combinational logic circuits

Abstract

Soft errors resulting from single-event upsets (SEUs) in combinational logic constitute an important and possibly dominant failure mode in future computing systems. State-of-the-art design methodologies are lacking in their ability to address the reliability challenges posed by SEUs in combinational logic in a cost-effective manner, and do not allow seamless exploration of the trade-offs between area-delay-power and SEU resilience.

This talk will describe our research efforts towards the design of SEU-resilient combinational logic circuits. The key ideas center around universal circuit-level models for logic gates, and their compatibility with conventional methodologies for area-power-delay-constrained design-space exploration. The universal circuit-level models are based on parameterized linear and generalized posynomial modeling techniques, and abstract away physical interactions between the ionizing particles and the substrate. Using these parameterized models, generic rank-and-optimize heuristics and global optimization algorithms can be applied to optimize one or more design parameters to improve design resilience to SEUs.

Biography

Kartik Mohanram received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay in 1998, and the M.S. and Ph.D. degrees in computer engineering from the University of Texas at Austin in 2000 and 2003 respectively. He is currently an assistant professor in the department of Electrical and Computer Engineering at Rice University, Houston, TX. His research interests include computer-aided design, simulation, and testing techniques for CMOS and emerging nanoelectronic technologies, low-power embedded systems, and parallelization for performance, low power, and dependability in next generation network servers. He serves on the program committees of the Intl. Conference on Computer-aided Design, the Intl. Test Synthesis Workshop, the Design Automation Summer School, the DAC Ph.D. Forum, and the ACM/SIGDA CADathlon.

Wednesday, Sep 28, 2005, ACES 2.402, 5 pm

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit
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