

**THE COMPUTER ENGINEERING RESEARCH CENTER  
THE VLSI SEMINAR SERIES**



**Todd Austin**

Associate Professor

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The University of Michigan, Ann Arbor

**Better Than Worst-Case Design**

**Abstract**

This talk introduces the audience to a novel design strategy, called "Better Than Worst-Case" design, which couples complex design components with simple reliable checkers. By delegating the responsibility of correctness and reliability to a checker, it becomes possible to quickly build designs that are capable of tolerating a variety of potential design disasters, ranging from functional design errors to circuit timing bugs. Two example designs are presented: DIVA and Razor. In addition, a complementary design technique, called typical-case optimization (TCO), is introduced as a way to take advantage of the relaxed design constraints on the core component.

The talk is intended for architects, designers and CAD engineers interested in novel techniques for robust design, their potential applications, and their implications to system design and CAD tools.

**Biography**

Todd Austin is an Associate Professor of Electrical Engineering and Computer Science at the University of Michigan in Ann Arbor. His research interests include computer architecture, compilers, computer system verification, and performance analysis tools and techniques. Prior to joining academia, Todd was a Senior Computer Architect in Intel's Microcomputer Research Labs, a product-oriented research laboratory in Hillsboro, Oregon. Todd is the first to take credit (but the last to accept blame) for creating the SimpleScalar Tool Set, a popular collection of computer architecture performance analysis tools. In addition to his work in academia, Todd is founder and President of SimpleScalar LLC and co-founder and Chief Technology Officer of BitRaker Inc and InTempo Design LLC. Todd received his Ph.D. in Computer Science from the University of Wisconsin in 1996.

**Thursday, Dec 8, 2005, ACES 2.402, 5 pm**

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit

<http://www.cerc.utexas.edu/vlsi-seminar/>