



THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

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Testing Chips, Masks, Processes: DFM and Test

Abstract

Test continues to evolve rapidly in response to technical and economic pressures. In fact, our ability to create new test and design for manufacturing methods are instrumental to the future of the semiconductor industry. From an EDA perspective, we see three major trends in the development of these methodologies. First, the use of on chip structures to aid test has led to the compression of test patterns by two to three orders of magnitude over traditional scan designs, with extremely low hardware overhead and virtually no loss of coverage. BIST takes this a step further. Second, manufacturing considerations have led to the need for more complex fault models. For example, delay faults arising from voids in Cu vias and wider parametric distributions, and bridging faults of interconnect both demand physical fault models. These physical phenomena lead to the third trend: the increased importance of diagnostics which allow designers to identify fault sites and possible fault causes, enabling faster yield ramps. Fault causes can be increasingly traced not only to the manufacturing process, but also to lithography and given design patterns.

In this talk we will focus on the questions of how design for manufacturing is affecting test and what test can do to help manufacturability and yield in the areas of process, lithography and design.

Biography

Dr. Raul Camposano joined Synopsys in 1994 and currently serves as Chief Technology Officer, Senior Vice President, and General Manager for the Silicon Engineering Group. He previously led the Design Tools business Unit from 1997 - 2000, in charge of Synopsys' entire suite of design tools. Prior to joining Synopsys, Raul was a Director for the German National Research Center for Computer Science, Professor of Computer Science at the University of Paderborn, and a Research Staff Member at the IBM T.J. Watson Research Center. Raul holds a B.S and M.S. in Electrical Engineering from the University of Chile, and a Ph.D. in Computer Science from the University of Karlsruhe. He has published over 70 technical papers and written and/or edited three books on electronic design automation. Raul is also an Advisory Professor at Fudan University and the Chinese Academy of Sciences and serves on numerous editorial and advisory boards. He was elected a Fellow of the IEEE in 1999.

Thursday, September 1, 2005, (ACE 2.402), 5 pm

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>