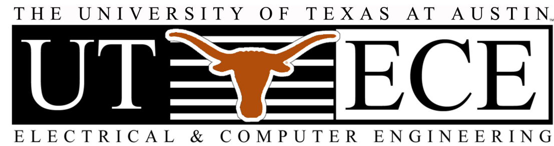

The Computer Engineering Research Center

The VLSI Seminar Series

Intel Distinguished Seminar

Ali Keshavarzi

Sr. Staff Research Scientist, Circuit Research Laboratories, Intel

Parameter Variation in Scaled CMOS Circuits

Abstract

Scaling of CMOS technology continues in spite of tremendous technology development barriers, design challenges and prohibitive costs. Today, the 65 nm CMOS technology node is moving from development to high volume manufacturing while research and development continues on future technology nodes including 45 nm, 30 nm and beyond. However, design of ICs in these scaled technologies faces growing limitations. It is increasingly difficult to sustain supply and threshold voltage scaling to provide the required performance increase, limit energy consumption, control power dissipation, and maintain reliability. These requirements pose several difficulties across a range of disciplines. On the technology front, the question arises whether we can continue along the traditional CMOS scaling path - reduce effective oxide thickness, improve channel mobility, and minimize parasitics. On the design front, researchers are exploring various circuit design techniques to deal with process variation and leakage. In my talk, I will try to introduce the challenges variation will pose to future scaling of CMOS technology, cover the components of variation and some circuit techniques to address threshold voltage and transistor parameter variation.

Biography

Ali Keshavarzi received his Ph.D. degree in electrical engineering from Purdue University, West Lafayette, Indiana. He is a senior staff research scientist at Circuit Research Laboratories (CRL) of Intel Corporation, Portland, Oregon. He is currently focusing on long-term research in low- power/high-performance circuit techniques and transistor device structures for future generations of microprocessors. Ali has been with Intel for thirteen years, has published more than 20 papers and has more than 30 patents (20 issued and the rest are pending patents). Ali has received the best paper award at 1997 IEEE International Test Conference at Washington, D.C. on testing solutions of intrinsically leaky integrated circuits. Ali is a member of the ISLPED and ISQED technical program committees.

Wednesday, September 7, 2005, ACES 2.402, 5 pm

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit
`http://www.cerc.utexas.edu/vlsi-seminar/`