



**THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES**

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Pre-layout wire-length predictions and applications

Abstract

In this talk I will introduce several structural metrics of netlists. I will demonstrate that those metrics can be used to predict which wires will be short after placement and routing. Such predictions can be applied to improve characteristics of the final layouts. I will show that clustering, placement, technology mapping, and decoupling capacitance insertion can benefit from the pre-layout information about wire-lengths.

Biography

Malgorzata Marek-Sadowska received an M.S. degree in Applied Mathematics and a Ph.D. degree in Electrical Engineering from Politechnika Warszawska (Technical University of Warsaw), Poland. From 1976 to 1982 she was an assistant professor at the Institute of Electron Technology at the Technical University of Warsaw. She became a research engineer at the U.C. Berkeley Electronics Research Laboratory in 1982 and continued there until 1990, when she joined the Department of Electrical and Computer Engineering at the University of California, Santa Barbara, as a professor. From 1993 to 1995 she was Editor-In-Chief of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. She is IEEE Fellow.

Monday, October 10, 2005, ACES 2.402, 5 pm

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>