



THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

Sandeep Kumar Goel

Philips Research Laboratories
Eindhoven, The Netherlands

On-Chip Test Infrastructure Design for High-Throughput Multi-Site Testing of SOCs

Abstract

Due to imperfections in the semiconductor manufacturing process, every IC needs to be tested for manufacturing defects. System chips (SOCs) are no exception to that. Manufacturing test of modern large SOCs requires expensive Automatic Test Equipments (ATEs) with large channel counts and very deep test-vector memory per channel. To reduce the test cost, multi-site testing is being employed, in which multiple instances of the same SOC are tested in parallel on a single ATE. More sites means more devices are tested in parallel. However, for a ATE with a fixed number of channels, large number of sites also means less ATE channels per SOC, which in turn increases the SOC test application time. Furthermore, a large number of sites also requires handling of more SOCs in parallel, which may increase the SOC handling time. Therefore, a large number of sites does not always result in a large test throughput. Hence, for a given ATE, instead of maximizing the number of sites, one should maximize the test throughput.

Efficient multi-site testing requires effective management of test resources like the on-chip test infrastructure (DfT), the number of ATE channels, and the vector memory depth per ATE channel, while taking into account parameters such as index time, contact yield, etc. In this talk, we focus on designing and optimizing on-chip test infrastructure (DfT), in order to maximize the test throughput for a given SOC and ATE. The on-chip DfT consists of an Enhanced-Reduced-Pin-Count-Test (E-RPCT) wrapper, and, for core-based SOCs, core wrappers and Test Access Mechanisms (TAMs). We present a two-step algorithm that designs the test infrastructure for a given SOC with a target ATE such that the SOC test-data volume fits on the target ATE within a single load and the test throughput is maximum. Finally, we present experimental results for the ITC'02 SOC Test Benchmarks and a complex Philips SOC.

Biography

Sandeep Goel received the B.Tech degree in Electronics Engineering from the Institute of Engineering and Technology, Lucknow, India, in 1998, the M.Tech degree in VLSI Design Tools and Technology from Indian Institute of Technology, Delhi, in 1999, and his Ph.D. degree in Electrical and Computer Engineering from the University of Twente, The Netherlands in 2005. Dr. Goel is a Member of the Scientific Staff at Philips Research Laboratories in Eindhoven, The Netherlands since 2000. His current research interests include Design-for-test (DfT) for core-based SOCs, silicon debug, BIST, test compression, multi-site testing, and test methodologies for power-aware designs. He has contributed chapters to two edited books, and published over 25 papers in journals and refereed conference proceedings. His paper on core-test wrapper design at the IEEE International Test Conference (ITC) 2000 was selected as one of the most significant papers presented at ITC in the last 35 years. He has several patents pending. He is currently serving on the program committees of the IEEE Infrastructure IP (IIP) workshop, and the IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS). He is a member of the IEEE and the IEEE Computer Society.

Monday, November, 7, 2005, ACES 3.418, 10:30 am

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit

<http://www.cerc.utexas.edu/vlsi-seminar/>