



THE COMPUTER ENGINEERING RESEARCH CENTER  
**THE VLSI SEMINAR SERIES**

**Tong Zhang**

Assistant Professor

Electrical, Computer and Systems Engineering Department  
Rensselaer Polytechnic Institute, Troy, New York

**Variation-Tolerant Signal Processing System Design in Sub-100nm  
Regime: A Case Study on Trellis Decoding**

**Abstract**

As CMOS technology is scaling down to sub-100nm regime, process and environmental variations have become one of the most crucial design challenges and may significantly jeopardize today and future integrated circuits (IC) energy and silicon area efficiency. Meanwhile, efficient signal processing IC implementations are of critical importance in the pervasive communication and computing era because of their ubiquity and significant impact on overall system energy and silicon cost. Certain unique features shared by most signal processing algorithms, together with the importance of efficient signal processing IC implementations, justify a domain-specific investigation on algorithm-based variation tolerance techniques for signal processing functions. Intuitively, the effectiveness of such domain-specific variation tolerance can be maximized by vertically integrating algorithm/architecture with physical level implementation. In this talk, we will present our recent work on pursuing cross-layer variation-tolerant signal processing system design methods. Motivated by the fact that variation-induced errors on different circuit logic signals may have largely different effects on the overall performance, we proposed an algorithm-based performance-centric unequal variation tolerance design framework, which is conceptually similar to the unequal error protection techniques being widely used in wireless image/video transmission. We will demonstrate its effectiveness using a case study on trellis decoders, which are being widely used in digital communication.

**Biography**

Tong Zhang joined Electrical, Computer, and Systems Engineering department at Rensselaer Polytechnic Institute as an assistant professor in 2002 after he got his doctoral degree from the University of Minnesota. He co-authored over 30 papers in the areas of VLSI architectures for error-correction coding, wireless communication base-band signal processing, and computer arithmetic, fault-tolerant system design for magnetic data storage and digital memory, and asynchronous IC design for signal processing. He won the Low Power Design Contest award at the 2005 International Symposium on Low Power Electronics and Design (ISLPED).

**Wednesday, October, 18, 2006, ACES 6.304, 5 pm**

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>