



THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

Soha Hassoun

Associate Professor, Department of Computer Science, Tufts University

finFETs: Thermal Modeling, Analysis, and Circuit Design

Abstract

As device dimensions shrink into the nanometer range, power and performance demands prohibit the longevity of traditional MOS devices in circuit design. A finFET, a quasi-planar double-gated device, has emerged as a potential replacement. A finFET is formed by creating a silicon fin which protrudes out of the wafer, wrapping a gate around the fin, and then doping the ends of the fin to form the source and drain.

We focus in this talk on finFET thermal and electrical issues. While finFETs provide promising electrostatic characteristics, they, like other ultra-thin body nano devices, have the potential to suffer from significant self heating. We propose a distributed thermal channel model use it to study the electro-thermal properties of multi-fin devices with both flared and rectangular channel extensions. We analyze variations in fin geometric parameters such as fin width and gate length, and we investigate the impact on thermal sensitivity using our thermal sensitivity metric, METS. We also report on gate sizing and independent gate biasing of finFET circuits. We show that finFET circuits are superior to 32nm circuits in performance, and in both dynamic and static power consumption.

Our work is novel because it provides the first thermal study of multi-fin devices and because it investigates thermally-aware finFET-based circuit design. Our thermal sensitivity metric is the first to capture device robustness to self-heating. Our finFET and 32nm bulk MOSFET circuit-level comparisons provide insight into future technologies. This work paves the way for future nanometer device and circuit-level design.

Biography

Soha Hassoun is currently an associate professor at Tufts University in the Department of Computer Science. She earned a Ph.D. from the Computer Science and Engineering Department at the University of Washington, Seattle, in 1997. Soha received a BSEE from South Dakota State University in 1986, and a Master's degree from MIT in 1988.

Dr. Hassoun's research interests include CAD, VLSI design, and computer architecture. Her current research focuses on finFETs, timing analysis for deep submicron circuits, and configurable computing for embedded systems. Prior to pursuing her Ph.D., Dr. Hassoun worked as a chip designer in the microprocessor design group at Digital Equipment Corporation. She was one of the 21064 Alpha processor's main circuit designers. She also designed a commercial cache controller for the VAX 6400, a vector processor, a 3-transistor dynamic RAM at MIT, and a router chip at UW. She spent January-July 2002 at IBM research labs in Austin working on a power estimation tool and some routing algorithms.

At Tufts, Dr. Hassoun teaches courses in CAD, Computer Architecture, and VLSI Design. Her teaching approach fosters critical thinking and design skills within classroom, lab, and homework activities. Dr. Hassoun serves on the advisory board for ACM's Special Interest Group on Design Automation (SIGDA). She has served as the program chair for the International Workshop on Logic Synthesis to be held in June 2001, and the general chair in 2002. She co-edited a book entitled, "Logic Synthesis and Verification". Dr. Hassoun is an NSF CAREER award recipient. In June 2000, she received the ACM/SIGDA Distinguished Service Award for creating the Ph.D. forum at DAC. Dr. Hassoun is a Tau Beta Pi Fellow. She is a member of ACM, a senior member of IEEE, and Eta Kappa Nu.

Friday, October, 20, 2006, ACES 2.402, 11 am

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit

<http://www.cerc.utexas.edu/vlsi-seminar/>