



THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES

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SOCIETY

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**Charge-Recycling MTCMOS: Circuit Techniques and Design
Automation Algorithms**

Abstract

Multi-threshold CMOS (MTCMOS) technology provides low leakage and high performance operation by utilizing high speed, low V_{th} transistors for logic cells and low leakage, high V_{th} devices as sleep transistors. Sleep transistors disconnect logic cells from the supply and/or ground to reduce the subthreshold conduction leakage currents in the sleep mode. One of the downsides of MTCMOS technique is the energy consumed during repeated transitions between the sleep and active modes of the circuit operation.

In my talk I will present a charge recycling MTCMOS technique that cuts the energy consumption for mode transitions in half while preserving the wakeup delay and reducing the ground bounce level in the target circuit. Tradeoffs related to the energy saving and leakage power increase of the charge-recycling vs. conventional MTCMOS will be discussed and related circuit optimization problems will be presented. I will conclude my talk by describing the application of the charge-recycling MTCMOS technique to row-based standard cell layouts.

Biography

Massoud Pedram received a B.S. in Electrical Engineering from California Institute of Technology in 1986 and M.S. and Ph.D. in Electrical Engineering and Computer Sciences from the University of California, Berkeley in 1989 and 1991, respectively. He then joined the Department of Electrical Engineering - Systems at the University of Southern California where he is currently a professor. Dr. Pedram is a recipient of the National Science Foundation's Young Investigator Award (1994) and the Presidential Early Career Award for Scientists and Engineers (a.k.a. the Presidential Faculty Fellows Award) (1996). His research has received a number of awards including two Best Paper Awards from the International Conference on Computer Design, two Design Automation Conference Best Paper Awards, and an IEEE Transactions on VLSI Systems Best Paper Award.

Dr. Pedram has served on the technical program committee of a number of conferences and workshops, including Design Automation Conference (DAC), Design and Test in Europe (DATE), Asia-Pacific Design Automation Conference (ASP-DAC), International Conference on Computer Aided Design (ICCAD), International Symposium on Low Power Electronics and Design (ISLPED), International Symposium on Physical Design (ISPD), and International Workshop on Logic Synthesis (IWLS). Dr. Pedram was a co-founder and general chair of the 1995 International Symposium on Low Power Design and the technical co-chair and general co-chair of the 1996 and 1997 International Symposium on Low Power Electronics and Design, respectively. He was the Technical Chair of the 2002 International Symposium on Physical Design and is the General Chair of the 2003 symposium. Dr. Pedram has given several tutorials on low power design at major CAD conferences and forums including, DAC, ICCAD, and ASP-DAC. He has published more than 250 journal and conference papers and written four books on various aspects of low power design.

Dr. Pedram is an IEEE Fellow and an ACM member. He serves on the Executive Committee of the IEEE Circuits and Systems Society (CASS) and on the Advisory Board of the ACM Special Interest Group on Design Automation. He is an Associate Editor of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. He received the 2000 Distinguished Service Award of ACM-SIGDA for contributions in developing the SIGDA Multimedia Monograph Series and organizing the Young Student Support Program. Dr. Pedram was a member of the Board of Governors of the IEEE CASS from 2000 to 2002 and the Chair of the Distinguished Lecturer Program of the IEEE CASS for 2003 and 2004. He is currently the CASS VP of Publications.

His research specializations include:

- Dynamic Power Management and Power-Aware Design
- Architectural and RT-Level Power Analysis, Design, and Optimization
- Ultra Low Power Circuit Design Techniques
- Smart Battery Design
- Physical Design Optimization and Logic Synthesis Techniques
- Design Automation Tools and Flows for Performance and Reliability Optimization of VLSI Circuits
- Signal Integrity Analysis and Optimization of VLSI Interconnects
- Power-Aware Sensor Networks

Thursday, November, 16, 2006, ACES 2.302, 5:30 pm

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>