



THE COMPUTER ENGINEERING RESEARCH CENTER
**IEEE CAS DISTINGUISHED LECTURE PROGRAM &
UT VLSI SEMINAR SERIES**

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High Performance Low Power VLSI Circuit Design

Abstract

This talk will start by analyzing the trade-offs between the two key metrics, power and performance, in modern digital circuits, and offer insights into ways to optimize the design by the proper setting of various design "knobs" such as V_{dd} , V_{th} , and sizing. The two-metric sensitivity-based optimization will then be expanded to multiple metrics, such as reliability, thermals, area, cost, etc., and will be followed by specific design methods for multi-threshold and multi-voltage circuits, adaptive circuit design using body biasing, temperature-aware design, optimal voltage scheduling, and bus encoding. The multi-threshold design methods will include a novel sleep mode state-preserving flip-flop, the multi-voltage circuit methods will include a single threshold high-performance low leakage circuit solution, the adaptive circuit design methods will include body-biasing schemes to compensate for thermal and aging effects, the optimal voltage scheduling scheme will explain why procrastination can actually save power for tasks with uncertain finishing times, while bus encoding can save power by reducing switching on global interconnect. This talk is the result of more than 100 publications, 6 patents, 8 PhD and 12 MS students, 12 years of academic and 8 years of industry experience.

Biography

Mircea R. Stan received the Ph.D. (1996) and M.S. (1994) degrees in Electrical and Computer Engineering from the University of Massachusetts at Amherst and the Diploma (1984) in Electronics and Communications from "Politehnica" University in Bucharest, Romania. Since 1996 he has been with the Department of Electrical and Computer Engineering at the University of Virginia, where he is now full professor. Prof. Stan is teaching and doing research in the areas of high-performance low-power VLSI, temperature-aware circuits and architecture, embedded systems, and nanoelectronics. He has more than eight years of industrial experience, has been a visiting faculty at UC Berkeley in 2004-2005, at IBM in 2000, and at Intel in 2002 and 1999. He has received the NSF CAREER award in 1997 and was a co-author on best paper awards at GLSVLSI 2006, ISCA 2003 and SHAMAN 2002. He was the chair of the VLSI Systems and Applications Technical Committee (VSA-TC) of IEEE CAS in 2006-2007, general chair for ISLPED 2006 and for GLSVLSI 2004, technical program chair for NanoNets 2007 and ISLPED 2005, and on technical committees for numerous conferences. He has been an Associate Editor for the IEEE Transactions on Circuits and Systems Systems I in 2004-2007 and for the IEEE Transactions on VLSI Systems in 2001-2003. He has also been a Guest Editor for the IEEE Computer special issue on Power-Aware Computing in December 2003 and a Distinguished Lecturer for the IEEE Solid-State Circuits Society (SSCS) in 2007-2008, and for the IEEE Circuits and Systems (CAS) Society in 2004-2005. Prof. Stan is a senior member of the IEEE, a member of ACM, IET (former IEE), and also of Eta Kappa Nu, Phi Kappa Phi and Sigma Xi.

Tuesday, December 9, 2008, ACES 2.402, 6:30–7:30 pm
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