

# UT VLSI SEMINAR SERIES

## **The Future of Design for Manufacturing**

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### **Abstract**

At 90nm and beyond, mask NRE and wafer costs have become major challenges to the proliferation of semiconductor technology and the overall economic health of the semiconductor industry. "Design For Manufacturing" (DFM) connects previously independent communities: product engineers, designers, lithographers, front-end processing, design IP and library suppliers, mask makers, and design automation tool providers.

In the past, DFM focused on catastrophic defect-limited yield (e.g., critical-area optimizations, and library optimizations for routability) as well as first-order solutions such as simple dummy fill rules for CMP. Today, DFM focuses on mask NRE costs, with first-order use of designers' intent to reduce OPC complexity, and on catastrophic yield characterization of design IP variants. Attention is also focused on prototyping of statistical performance analysis methodologies, and on infrastructure and standards to enable bidirectional communication between the design and process worlds. What does the future of DFM hold? Two examples (we'll discuss quite a few!) are the following.

- (1) Today's post-tapeout functionality (e.g., OPC and CMP fill) will move up the design flow to interact more closely with synthesis, timing optimization, and place-and-route - and will become more explicitly driven by chip metrics such as leakage power or reliability.
- (2) As control of process variability becomes less manageable in future technology nodes, DFM will be driven more directly by parametric yield and cost objectives. For example, future DFM tools will center designs for maximum manufacturing robustness in order to minimize over-design and lithography costs.

### **Biography**

Since 1997, Andrew B. Kahng's research in VLSI Design for Manufacturing has pioneered methods for automated layout for alternating phase-shift masks, dummy fill synthesis for CMP, parametric yield-driven and variation-aware OPC, fracturing for mask data preparation, and reticle plan and wafer optimizations. He served as founding General Chair of the International Symposium on Physical Design, and technical program co-chair of the 2004 and 2005 Design Automation Conferences. From 2000 through 2003, he chaired the U.S. and international working groups for Design technology for the ITRS roadmap. His recent research focuses on the VLSI design-manufacturing interface, and on physical design and performance analysis of VLSI. As of October 2004, Dr. Kahng is on leave of absence from UCSD, serving as chairman and CTO of Blaze DFM, Inc.

*Coffee and cookie will be served. For more information about the UT-Austin VLSI Seminar Series, please visit the web. <http://www.cerc.utexas.edu/vlsi-seminar/>*