U T V L S I S E M I N A R S E R I E S

Exploiting Level Sensitive Latches in Wire Pipelining

Prof. Jiang Hu
EE Department, Texas A&M University

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Abstract

Wire pipelining emerges as a new necessity for global wires due to increasing wire delay, shrinking clock period and growing chip size. Existing approaches on wire pipelining are mostly based on edge triggered flip-flops. In this presentation, we demonstrate the advantages of using level sensitive latches in terms of both latency and area cost. The input-output timing coupling and the strict short path constraint for latches demand additional design elaborations compared with flip-flops. New approaches are proposed to solve these difficulties so that the advantages of latches can be fully utilized. In particular, a deferred delay padding technique is developed to correct short path violations with the minimal extra cost. These techniques are integrated with a dynamic programming based concurrent synchronous element and repeater insertion framework. Experimental results confirm the advantages of using latches as well as effectiveness of our algorithms.

Biography

Jiang Hu received the B.S. degree in optical engineering from Zhejiang University in 1990, the M.S. degree in physics and the Ph.D. degree in electrical engineering from the University of Minnesota in 1997 and 2001, respectively. From 2000 to 2002, he was with IBM Microelectronics Division where he received an IBM First Plateau Invention Award and four U.S. patents. Currently he is an assistant professor in the Department of Electrical Engineering at the Texas A&M University. His research interest is on Computer-Aided Design for VLSI circuits, especially on interconnect optimization, clock network synthesis, variation tolerant design, power efficient physical design and design for manufacurability. Dr. Hu received a best paper award at the ACM/IEEE Design Automation Conference in 2001. He has served in technical program committees of ICCD, ISPD, ISCAS, ICCAD and DATE.

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