

Sub-Lithographic Semiconductor Computing Systems

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Abstract

How Can We Build Nanometer Scale Computing Devices?

Enabled by advances in our basic scientific understanding at the molecular and atomic scales, we can now engineer designed nanostructures without using lithography. Key features can be a few nanometers wide -- a few silicon atoms wide, perhaps the ultimate scale for devices. This allows us to design computing components without the costs or limits of ultra-fine lithography. Design at this scale, however, will not simply be an extension of our familiar VLSI design. We may not be able to directly pattern complex features, but rather must exploit basic physical properties to define feature sizes, self-assembly to create ordered devices, and post-fabrication reconfigurability to define functionality and mask defects. This creates new challenges for design and exposes a different cost structure which motivates different computing architectures than we found efficient in conventional, lithographically patterned silicon. I will review the emerging nanoscale fabrication building blocks, sketch a hybrid fabrication scheme which uses these building blocks along with lithography, and present a plausible architecture for nanoscale electronics based on silicon nanowires. I demonstrate that these nanoscale constructs are sufficient to provide universal logic functionality with all logic and signal restoration operating at the nanoscale.

Biography

André DeHon is currently an assistant professor in Computer Science, California Institute of Technology. He received his B.S., M.S. and Ph.D. all from Massachusetts Institute of Technology in 1990, 1993, and 1996, respectively. His research areas include Physical implementation of computation, including physical substrates (VLSI, molecular, etc.), programmable media (FPGAs, processors), mapping (compilation, CAD), system abstractions and dynamic management (run-time systems, operating systems, scheduling), and problem capture (programming languages).

Coffee and cookie will be served. For more information about the UT-Austin VLSI Seminar Series, please visit the web. <http://www.cerc.utexas.edu/vlsi-seminar/>

