



THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES

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Insights into Fast Physical Synthesis

Abstract

In modern VLSI designs, traditional design flows break during chip layout due to the lack of interaction between synthesis and the physical design stages. Consequently, over the last few years, a new type of design optimization called *physical synthesis* has become essential for realizing a physically and electrically correct design that meets the timing specification. Physical synthesis combines placement, gate sizing, buffer insertion, logic transforms, and routing all in a single automated algorithm. Managing the complexity of the interaction between the different phases is a major challenge. This talk surveys IBM's physical synthesis tool called PDS and highlights some of these challenges. It also describes some new techniques that have emanated from the PLATO project, a research effort that seeks super fast techniques for performing physical synthesis.

Biography

Charles J. Alpert received the B.S. degree in Math and Computational Sciences and the B.A. degree in History from Stanford University in 1991. He received the Ph.D. degree in Computer Science from UCLA in 1996. He currently works as a Research Staff Member at the IBM Austin Research Laboratory, where he serves as the team lead for the PLATO project. PLATO is a physical synthesis tool designed for fast floorplan evaluation and timing closure.

Charles has over 70 conference and journal publications and has thrice received the Best Paper Award from the ACM/IEEE Design Automation Conference. Charles has served as the general chair and the technical program chair for the Tau Workshop on Timing Issues in the Specification and Synthesis of Digital Systems and the International Symposium on Physical Design. He also serves as an associate editor of IEEE Transactions on Computer-Aided Design. For his work in mentoring SRC funded research, he received the Mahboob Khan Mentor Award in 2001.

Wednesday, February 2, 2005, ACES 2.402, 5 pm

**Coffee and cookie will be served. For more information about the VLSI Seminar Series,
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