



**THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES**

Andrew Kennings

Associate Professor of Electrical and Computer Engineering
The University of Waterloo, Waterloo, Canada

Understanding Force-directed Placement

Abstract

Force-directed placers are an attractive approach for placement and are of interest for several reasons. Large standard cell and mixed-size problems are handled seamlessly by such methods. Furthermore, force-directed placers provide continuous trajectories for cell locations and therefore seem quite amenable to timing- and congestion-driven placement, physical re-synthesis, and so forth. Unfortunately, research literature offers little information pertaining to the actual implementation details of a force-directed placer; i.e., only high-level algorithmic descriptions are provided and no open-sourced implementations are available that facilitate a “self-discovery” of this technique. Finally, few comparisons to other placers (e.g., academic min-cut tools) are available, making it difficult to judge the capability of force-directed methods to produce high-quality placements.

This talk will present some of the implementation details of an open-source, force-directed placer developed at the University of Waterloo. Problems (and accompanying solutions) discovered while developing the placer will be presented. Methods to improve the quality of placements (measured in terms of wire length) produced by force-directed methods will also be presented. Comparisons with other leading academic tools will be provided using both standard cell and mixed-size problems. Other currently-active research into these methods will also be presented.

Biography

Andrew Kennings received the BSc, MSc and PhD degrees in Electrical Engineering from the University of Waterloo in 1992, 1994, and 1997, respectively. Presently, he is an Associate Professor of Electrical and Computer Engineering at the University of Waterloo, Waterloo, Canada. Prior to joining the University of Waterloo in 2002, he worked as a Staff Software Engineer in the Data Communications Division at Cypress Semiconductor where he worked on technology mapping, placement, routing and timing analysis for programmable logic devices. Current research interests include VLSI CAD, with particular emphasis on placement algorithms for ASIC and FPGA technologies.

Thursday, February 24, 2005, ACES 2.402, 5 pm

**Coffee and cookie will be served. For more information about the VLSI Seminar Series,
please visit <http://www.cerc.utexas.edu/vlsi-seminar/>**