



THE COMPUTER ENGINEERING RESEARCH CENTER  
THE VLSI SEMINAR SERIES

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**Simulating Boolean Functions: Hyperlinear Structures and Symmetry**

**Abstract**

Since simulation tends to be the most time consuming part of any VLSI design, researchers have continually sought faster and faster techniques for simulating circuits. One obvious method for improving simulation speed is to combine several gates into a single Boolean function and simulate the function as a unit. Unfortunately, this is much easier said than done. In most cases the technique for simulating the function is more time consuming than simulating the original collection of gates.

The hyperlinear technique permits functions to be simulated in roughly the same amount of time as a single gate. The function is represented as a state machine and changes in the inputs are used to change states. Metamorphic programming techniques are used to provide an efficient simulation of the state machine. In the worst case, the function is represented as a hypercube, but symmetries in the function can be used to reduce the number of dimensions in the hypercube while expanding the cube along another dimension. As the number of dimensions is reduced, the efficiency of the simulation increases. In the ideal case, the hypercube is collapsed into a linear state machine with  $n$  inputs and  $n + 1$  states. Many types of symmetry can be used for the collapse: total and partial symmetries, skew symmetries, and conjugate symmetries. The hyperlinear technique is unique in its ability to handle skew symmetries and conjugate symmetries. Skew-symmetric functions are those that are symmetric with one or more inputs inverted with respect to the others. Conjugate symmetries are similar to skew symmetries, but with certain inputs conditionally inverted by others. Work is underway to exploit other types of symmetry as well.

**Biography**

Peter M. Maurer is an Associate Professor of Computer Science at Baylor University. His research interests include component-level programming, VLSI design, Computer architecture, and Parallel processing. Maurer received a PhD in Computer Science from Iowa State University. He was with Bell Laboratories as a member of their technical staff from 1982-1987. He was a member of the faculty of the University of South Florida, Tampa from 1987-2002. In the fall of 2002, he joined the faculty of Baylor University, Waco, TX. He has served as an Associate Editor for *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.

**Friday, March 11, 2005, ACES 6.304, 11 am**

**Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>**