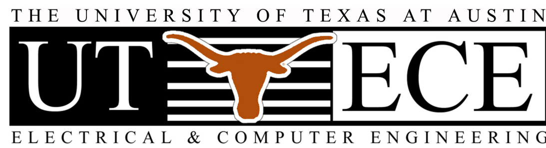

THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

Shalini Ghosh
Electrical and Computer Engineering
The University of Texas at Austin

Reducing Power Consumption During Fault-tolerant Computing and Offline Testing

Abstract

In this talk, I will discuss different techniques for power reduction in fault-tolerant computing with concurrent error detection and offline circuit testing. Power management is critical in both these domains, since high power dissipation during testing or concurrent error detection can drive up production cost and even cause errors.

The first part of the talk focuses on power reduction for fault-tolerant systems with concurrent error detection, where errors in operation of the circuit are detected (and possibly corrected) at normal operational run-time. Fault-tolerant circuits with on-chip hardware for error detection and correction are important in mission-critical applications, where dependability of the system and integrity of the data are critical. In fault-tolerant computing environments, power dissipation has lately become a first-order design criterion, due to the significant hardware overhead for detecting/correcting errors and ensuring system reliability. I will present two problems that illustrate the benefit of reducing power in concurrent error detection: (1) error correcting codes for memory checkers; (2) synthesis of parity prediction circuits.

The next part of the talk will discuss power reduction for offline testing, which is one of the most expensive stages of the VLSI circuit design cycle. With the advent of high-performance and low-power devices, the power consumed during circuit testing has become a critical issue. It has been observed that the power dissipated in a circuit during the testing phase can be much larger than the power consumed during normal operations. I will present techniques for reducing power in two popular methods of offline circuit testing: (1) scan testing; (2) built-in self-test.

Finally, I will discuss why fault tolerance and testing are becoming increasingly important in nano-scale devices.

Biography

Shalini Ghosh is currently a Ph.D student in the department of Electrical and Computer Engineering at the University of Texas at Austin. She received her M.S. from the Computer Engineering Department of University of California at Santa Cruz (UCSC). At UCSC, she worked with the Semiconductor Test Group on VLSI Testing.

Her research interests are in power optimization for fault-tolerant and dependable systems, concurrent error detection, system reliability, VLSI testing, design for testability, fault modeling, and architecture validation. She plans to continue research on low power fault tolerance and testing, and explore fault tolerance issues in nano-scale devices and sub-micron architectures.

Wednesday, April 6, 2005, ACES 2.402, 5 pm

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit
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