



**THE COMPUTER ENGINEERING RESEARCH CENTER
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**The Design and Implementation of a First-Generation CELL Processor:
A Multi-Core SoC**

Abstract

This paper describes the design and implementation of a first generation CELL Processor. The processor is a multi core SoC consisting of a 64 bit Power Architecture Processor Element (PPE) with an associated L2 memory subsystem, multiple Synergistic Processor Elements (SPE) each with its own local memory (LS), a high bandwidth internal Element Interconnect Bus (EIB), two configurable non-coherent I/O interfaces, a Memory Interface Controller (MIC), and a Pervasive unit that supports extensive test, monitoring, and debug functions. The design has roughly 234 million transistors implemented in 90nm SOI technology with 8 levels of copper interconnects and one local interconnect layer. The chip is designed with a high degree of modularity and reuse to maximize the custom circuit content and achieve a high frequency clock rate. The chip has been tested at various temperatures, voltages, and frequencies. Correct operation has been observed in the lab on first pass silicon at frequencies well over 4GHz.

Biography

Dac C. Pham joined IBM in 1987, where he worked on IBM's 386SX, 386SLP, and Blue Lightning family of processors (an X86 compatible architecture). In 1992, he joined the Apple-IBM-Motorola's Somerset Design Center, where he worked on IBM's PowerPC 603 and follow-on processors which lead to PowerPC G3. In 1997, he joined the IBM's Giga-Processor team where he worked on IBM's Power 4 processor which was used in IBM servers and Apple's G5. Between 1999 and 2003, he was with Intel's Texas Design Center and managed the Chip Implementation team of a high speed next generation Pentium processor. He re-joined IBM in 2003, where he worked on the high speed, multi-core, broad band first-generation CELL processor. Dr. Pham is currently the Sony-Toshiba-IBM Design Center Chief Engineer and Global Convergence Manager.

Wednesday, April 20, 2005, AVAYA Auditorium (ACE 2.302), 5 pm
Coffee and cookie will be served. For more information about the VLSI Seminar Series,
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