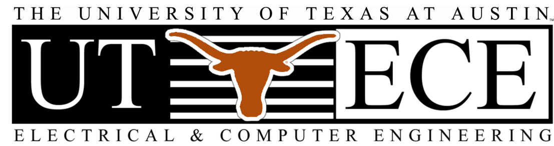

THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

Dr. Thomas W. Williams
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Boulder, Colorado

Design For Testability: The Path to Deep Submicron

Abstract

Design has never been simple, but at 130 nm and below–and definitely at 90 nm–it is becoming increasingly difficult. Process and lithography issues continue to drive our advance to new technology nodes. Due to the effects of scaling, defect mechanisms are no longer easily identified with single ”stuck at” fault models but rather are demanding far more complex and challenging solutions. For example, shorts are now being extracted from the physical layout of a design, with special tests being created to detect them. But this is just the beginning; delay testing of all transition faults is now a new objective of design for testability (DFT). New demands are being made on design to not only create the correct function and help with testing but also to help yield ramp-up. The area of design for manufacturing (DFM) and design for yield (DFY) are now also talking hold as new requirements for design. Manufacturing and test are beginning to develop an even stronger relationship due to the close interconnection between yield ramp-up and diagnostics, which are supported by DFT structures included in the design.
In this presentation, Dr. T. W. Williams addresses these current challenges in the area of design for testability, manufacturing, yield, and diagnostics. In addition, he will discuss the future challenges facing designers, and the new tools and methodologies which the design community will be dealing with.

Biography

Dr. Thomas W. Williams is a Synopsys Fellow at Synopsys in Boulder, Colorado, U.S.A. Formerly he was with IBM Microelectronics Division and manager of the VLSI Design for Testability group. He received a BSEE from Clarkson University, an M.A. in pure mathematics from the State University of New York at Binghamton, and a Ph.D. in electrical engineering from Colorado State University. He has received numerous best paper awards from the IEEE and ACM, is the founder or co-founder of a number of workshops and conferences dealing with testing, and was twice a Distinguished Visitor lecturer for the IEEE Computer Society. Williams has previously served on the Computer Society Board of Governors and the IEEE Board of Directors, and was the society’s 2000 Treasurer. He is a member of the, Eta Kappa Nu, Tau Beta Pi, IEEE, ACM, Sigma Xi, and Phi Kappa Phi. In 1985 and 1997, he was a Guest Professor and Robert Bosch Fellow at the Universitaet of Hannover, Hannover, Germany. Dr. Williams was named an IEEE Fellow in 1988 and received the Computer Society’s W. Wallace McDowell Award for outstanding contributions to the computer art in 1989.

Wednesday, February, 1, 2006, ACES 2.402, 5 pm

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit
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