



THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES



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Austin

Impact of Variability on Power

Abstract

The advent of the 100+ Watt chip threatens to derail the long standing performance gains we have been counting on from technology scaling according to Moore's law. Phenomena such as leakage and technology-induced variability further worsen this trend. This has been contributed to by a design methodology which emphasizes performance (frequency) at all costs and all but ignores power dissipation. The industry is now in desperate need for a power-oriented design methodology which treats power as a first class objective, and that allows designers to make power/performance and power/area trade-offs at the micro-architectural, circuit, and even technology levels. This talk will address one small part of this need, namely the interaction between and analysis of the manufacturing variability and power.

Biography

Sani received his PhD from Carnegie-Mellon university in the eighties. He worked for ten years at Bell Laboratories on various aspects of design and technology coupling including device modeling, parameter extraction, worst case analysis, design optimization and circuit simulation. He joined the IBM Austin Research Laboratory in January 1996 where he is presently managing the tools and technology department, which is focused on design/technology coupling and includes activities in: model to hardware matching, simulation and modeling, physical design, statistical modeling, statistical technology characterization and similar areas.

Friday, March, 3, 2006, ACES 2.302 (Avaya Auditorium), 4 pm
Coffee and cookie will be served. For more information about the VLSI Seminar Series,
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