



THE COMPUTER ENGINEERING RESEARCH CENTER  
**THE VLSI SEMINAR SERIES**

**Dileep Bhandarkar**

Director, Enterprise Architecture Lab  
Intel

**Multi-Core Microprocessor Chips: Motivation & Challenges**

**Abstract**

Advances in semiconductor process technology allow hundreds of millions of transistors to be integrated on a single chip. Intel's 90 nm technology Montecito chip was the first Billion transistor chip featuring dual cores and large cache in 2005. Nanotechnology that continues to drive Moore's Law provides a doubling of the transistor density every two years. Multi-core chips will become common not only in high end servers but also in desktop and mobile PCs.

Multi-core processors present several challenges related to on-chip system architecture, power management, reliability, and software scaling. This talk will touch upon some of these challenges and discuss some possible solutions.

**Biography**

Dr. Bhandarkar is an IEEE Fellow, and a Distinguished Alumnus of the Indian Institute of Technology, Bombay, where he received his B. Tech in Electrical Engineering. in 1970. He also has a M.S. and Ph.D. in Electrical Engineering from Carnegie Mellon University, and has done graduate work in Business Administration at the University of Dallas.

He is currently Director of the Enterprise Architecture Lab in processors and chipsets. He has been with Intel since 1995 and has managed system architecture and performance analysis activities. Prior to joining Intel, he spent almost 18 years at Digital Equipment Corporation, where he managed processor and system architecture, and performance analysis work related to the VAX, Prism, MIPS, and Alpha architectures. He also worked at Texas Instruments for 4 years in their research labs in a variety of areas including magnetic bubble memories, charge coupled devices, fault tolerant memories, and computer architecture.

Dr. Bhandarkar holds 15 U.S. Patents and has published more than 30 technical papers in various journals and conference proceedings. He is also the author of a book titled Alpha Architecture and Implementations.

**Wednesday, May, 3, 2006, ACES 2.302, 2 pm**

**Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>**